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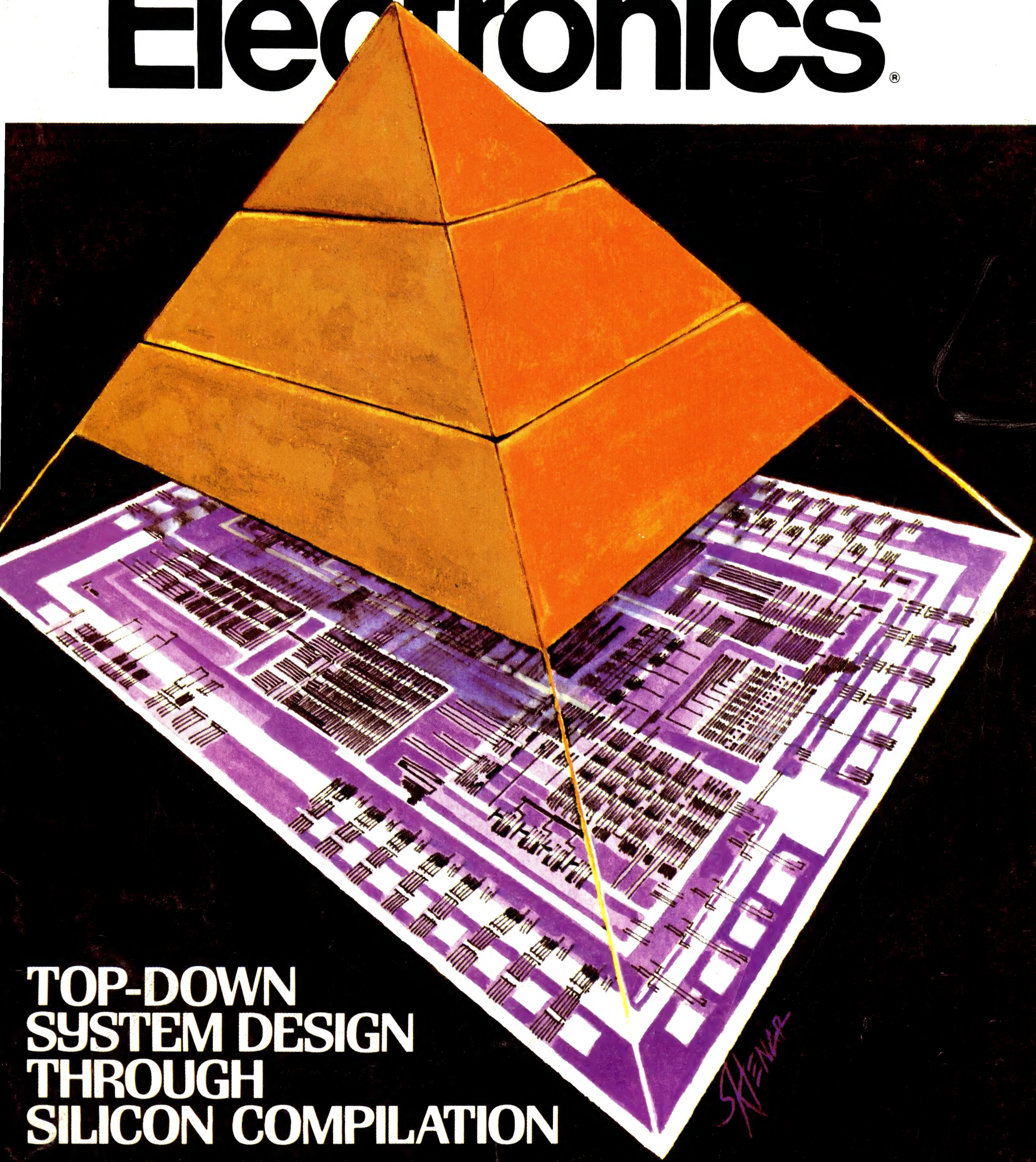

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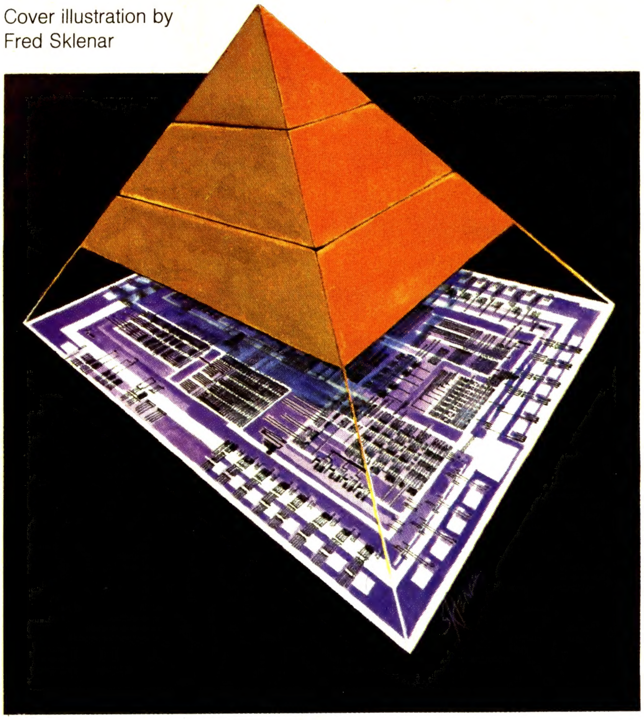
Cover illustration by
Fred Sklenar



The Cover Story

Top-down system design through silicon compilation

Integrated technology *drastically reduces time and manpower requirements for designing very large-scale integrated circuits—without sacrificing performance or the efficient use of chip real estate*

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Highlights

Route 128 companies exhibit mixed feelings at Electro time, 99

Executives at electronics companies with headquarters along Massachusetts' Route 128, the high-tech highway running through Boston's western suburbs, will show up at Electro/84 in exuberant moods: right now, business is booming. However, the short-term outlook belies some long-term concerns about the effect on high-tech industries of moves by the state government on taxes and by the federal government on export controls.

The arrival of VLSI gives C-MOS an attractive new look, 129

The 1980s have brought much new attention to complementary-MOS technology and its application in new products. Traditionally, the advocates of C-MOS have praised its low power dissipation, large noise margins, and simple, ratioless design. With the arrival of very large-scale integration, these advantages mean more than ever.

A standard is proposed for wideband local networks, 145

Most people are not aware of the steps now being taken to standardize local-network protocols and connections for mainframes and supercomputers. The American National Standards Committee has drafted a standard that is close kin to three commercial products now on the market. Its action will spur the development of custom large-scale integrated parts and promote competition in the marketplace. As a result, current prices for wideband networks are bound to drop significantly.

What's ahead. . . .

Data-base systems: Besides tackling the issues that surround data-base systems for microcomputers, a special report will look at the role these systems will play in the coordination and control functions of the future. It will also take a peek at natural-language user interfaces based on artificial-intelligence technology, which will complement data-base systems. . . .**May 17.**

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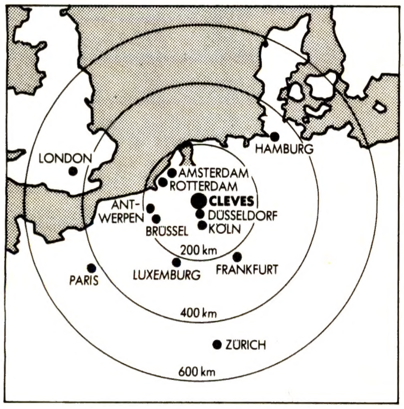

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Editor's letter

This year, the annual regional convention and exhibit known as Electro occurs in the centennial year of the Institute of Electrical and Electronic Engineers, the show's patron. On such an occasion, we think it behooves us to take a moment to reflect on the importance of this organization to the profession and to the industry.

Despite the rise of some dissidence and attendant controversy about the role of the IEEE in advancing the economic and social status of its membership, no one can dispute the tremendously beneficial service it has rendered in its traditional activity of establishing standards and disseminating important technical publications, and through its many conferences and seminars, providing forums for presentation and discussion of technical innovations. In all of these activities, the standards of the institute have been consistently high, and this has contributed in no small measure to the astonishing technical progress the industry has made and continues to make.

As part of the centennial year celebration, the IEEE has recently published an interesting book entitled "Engineers and Electrons," a combined history of the electrical engineering profession and of the society. It was written by John D. Ryder and Donald G. Fink, whose distinguished careers have long linked them with the electronics industry and with the IEEE. Ryder, a prominent academic figure, was head of the EE department at the University of Illinois and later Dean of Engineering at Michigan State University. Fink, who was editor of this magazine from 1946 to 1952, was the first general manager of the IEEE after it was formed out of the merger of the old IRE and AIEE organizations.

Replete with many fascinating illustrations of the imporant inventions and developments in electronics over the last two centuries (but with emphasis on the last 100 years) and the people behind them, the writing is at a popular, relatively nontechnical level, which makes the book suitable for the casual as well as the technically informed reader. While one can quibble with the relative allotment of space to various topics, the writing is uniformly straightforward and very crisp and lively for a book of this kind. It seems to us that more space should have been allotted to computers and semiconductors, and perhaps somewhat less to television, although the account of the competition between the CBS field-sequential system and RCA's compatible-color system is fascinating. That this priority exists isn't surprising, since Don Fink was a member of the National Television Standards Committee, which developed today's color standards, and has written several books on the subject.

Each chapter in the book ends with a list of references for further reading, and this leads to the one major bone we must pick with the authors. Although early on they describe and credit *Electronics*' role in the derivation of the generic term "electronics" for the industry and its associated technologies, we looked in vain for any reference to our own history of the electronics industry, produced in an issue to commemorate our 50th anniversary in April 1980 and later published as a book, "An Age of Innovation." That aside, we can recommend "Engineers and Electrons" as a worthy addition to the library of anyone interested in the ongoing dynamic history of the field of electronics.

As for Electro itself, since this year the venerable convention and show is set in Boston, we thought it appropriate to take an in-depth look at one of the great electronics technology centers of the U. S: the industrial complex surrounding the city in that belt known as Route 128. We dispatched Karen Berney of our Washington bureau to see how this bustling high-technology community is faring in these volatile times. She discovered that optimism runs high for increased prosperity in this Silicon Valley East, yet there is an undercurrent of serious concern over local and national political policies that could derail much of the economic progress that executives are anticipating. You'll find her story beginning on p. 99. ☐

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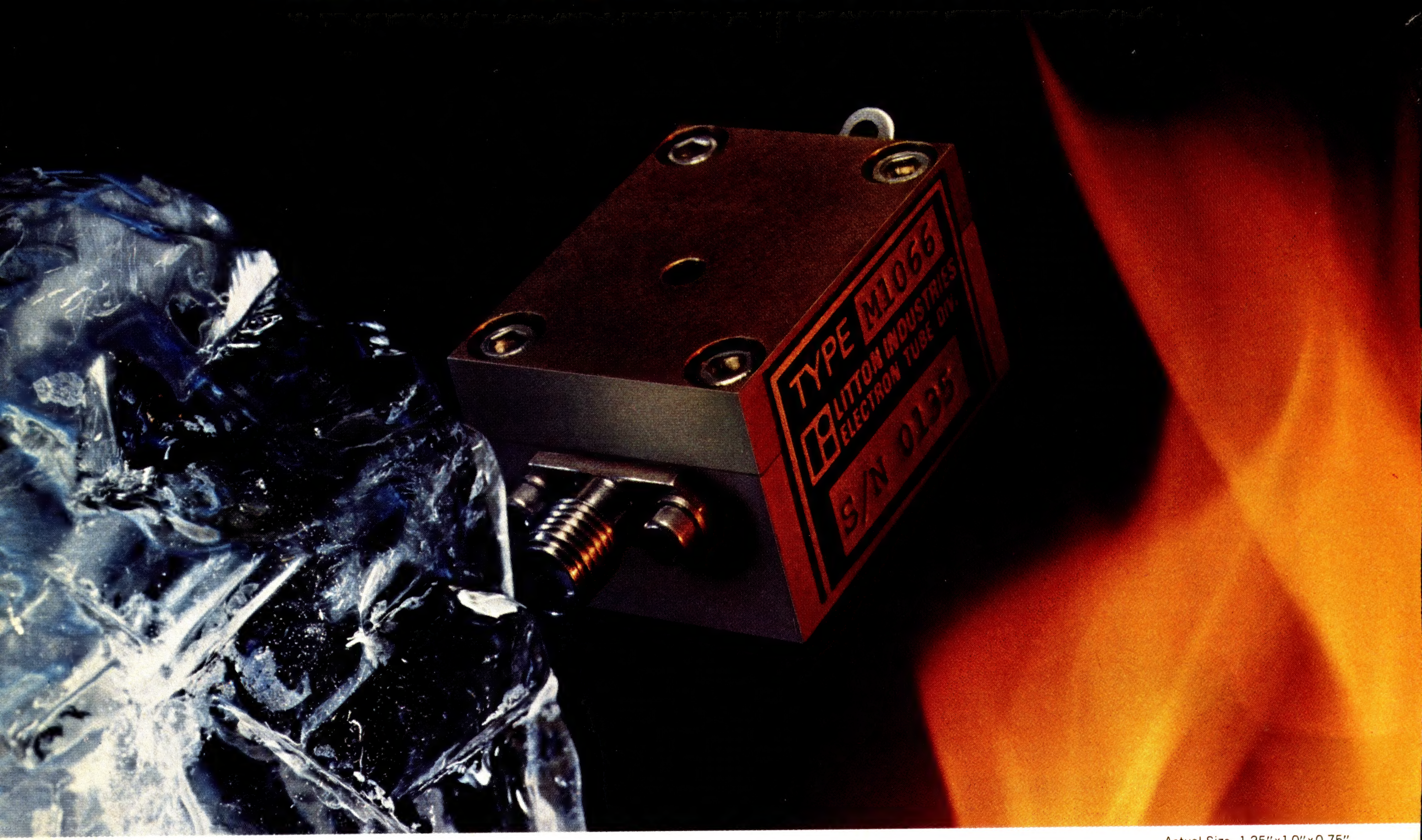

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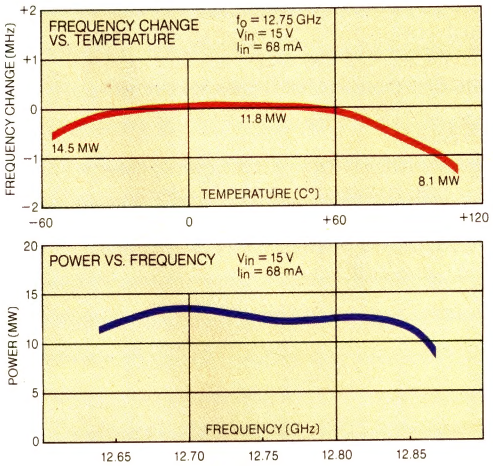

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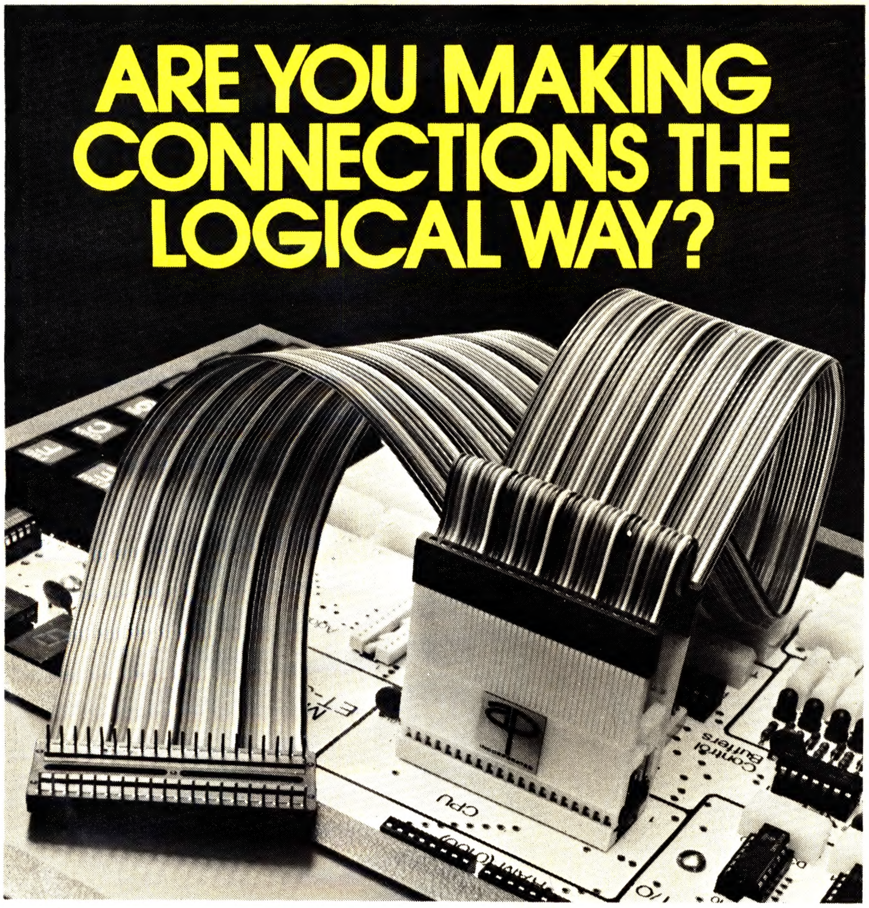

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Electro Booth #1445

'Readers' comments

The home of the brave

To the Editor: I quite agree with Irwin Feerst and the Committee of Concerned EEs (Readers' comments, "Embattled EEs," March 8, p. 8) that the willingness of this country's corporations to hire foreign graduates of U. S. universities "undercuts the economic security of all American technical professionals." Surely these alien graduates should be encouraged to leave this country; to take their academic degrees (mere pieces of paper), their publications, their patents, their Nobel Prizes (mostly in such esoteric subjects as genetics and the origins of the universe), their many giant companies (Wang, Intel, Tandon, and the rest), their many small companies (which are too numerous to mention), and their bright-eyed children (espcially those who have won Westinghouse Fellowships); and to return to those places whence they came.

We American professionals would then be able to live in the land of the free and the home of the brave—with no competition from foreigners to turn us into cowards—and to enjoy a life of leisure and fat salaries at the expense of the American consumer. Better still, why not totally avoid the economic insecurity foreigners create and refuse to let the alien students into these U. S. universities in the first place? As a fringe benefit of refusing them admission, even American graduate students will share in the joys of working in the land of the free and the home of the brave.

Prabjit Singh, Ph. D.
Poughkeepsie, N. Y.

A correction

A headline in the issue of Feb. 23 ("Honeywell adds another VHSIC-technology part for the commercial market," p. 42) incorrectly implied that Honeywell Inc.'s HE2000 is a "VHSIC-technology" part. In fact, however, the device will be built with a forerunner of Honeywell's process for the Defense Department's Very High-Speed Integrated Circuits Program.

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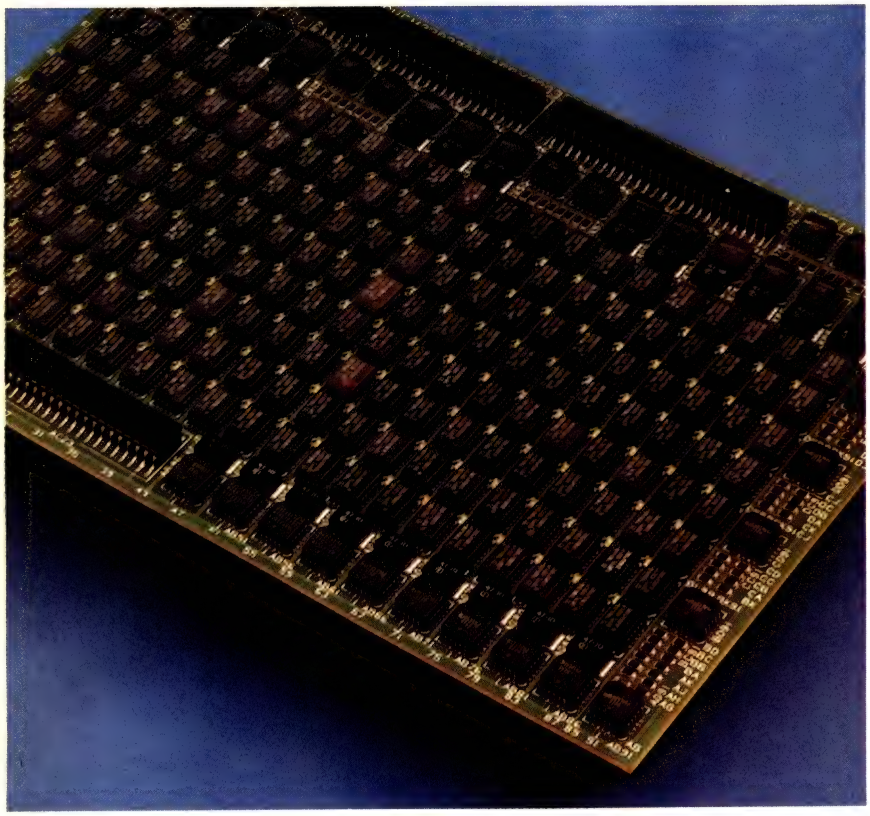


Avoiding stress in surface-mounting MLC chips

The most critical factor in surface mounting multilayer ceramic chip capacitors, thermal shock, can be avoided by preheating the capacitors before they contact the solder. Figure 1 indicates the ideal temperature profile for wave soldering MLC chips.

Temperature Guidelines

As the chart shows, the ideal guideline for preheating is to raise the chip temperature at a rate of approximately 2°C per second to within 100°C of the solder bath. Although the preheat rate is important, the more critical parameter is the differential between chip and solder temperatures when the two meet. The closer these two temperatures, the less likely there will be thermal shock.

Wave Soldering

Figure 2 charts the internal temperature of an MLC chip during a single-wave-soldering operation. The ceramic chip is mounted on the bottom side of the board with an imbedded thermocouple. Although the rate of increase in the capacitor temperature is 4.5°C/sec., no thermal shock is observed, since the capacitor is brought to within 50°C of its peak temperature in the solder wave.

Preferred Wave Solder Profile for Ceramic Chip Capacitors

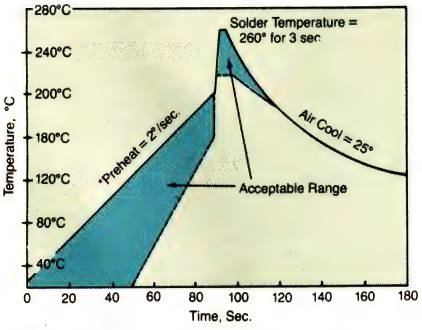
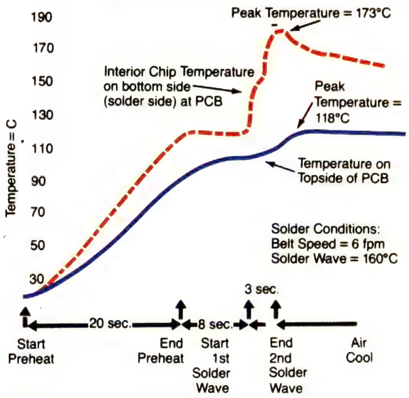


Fig. 1

Fig. 2 Internal MLC Chip Temperature During Wave Soldering to PCB



Discussion

Bottom-sided (solder-side) soldering results in critical temperature differentials between PC board and chip, as shown by comparing chip with board temperature using an additional thermocouple mounted on a copper runner on the top side of the board. Here peak board temperature was 118°C versus a chip temperature of 173°C when coming into contact with a 260°C solder wave for 3 sec.

AVX results show that the cooling cycle is as important as the preheat cycle. Gradual cooling not only avoids thermal shocking of the capacitor, but also allows relaxation of thermal stress in the solder and boards.

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AVX Technology For The Times

Photo: This experimental circuit board from Texas Instruments shows the surface mounting technique. The board is not an available commercial product.

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The Pentagon should keep its hands off publication rights

The Department of Defense has for some time been conducting an offensive that amounts to a full-scale attempt to smother the academic tradition of full and open communication about scientific and technological innovation. It has been doing so in a misguided attempt to keep unclassified material that it deems militarily sensitive from reaching the Soviet Union.

Now the Pentagon has pushed another spearhead into the battle: it wants to control the publication of research papers in certain fields. That action has elicited a cry of anguish from the presidents of the California Institute of Technology, Stanford, and the Massachusetts Institute of Technology, whose protest took the form of a letter to Under Secretary of Defense Richard DeLauer. The letter pointed out that the latest provision, approved by an internal Defense Department committee, goes far beyond what the universities had been willing to accept.

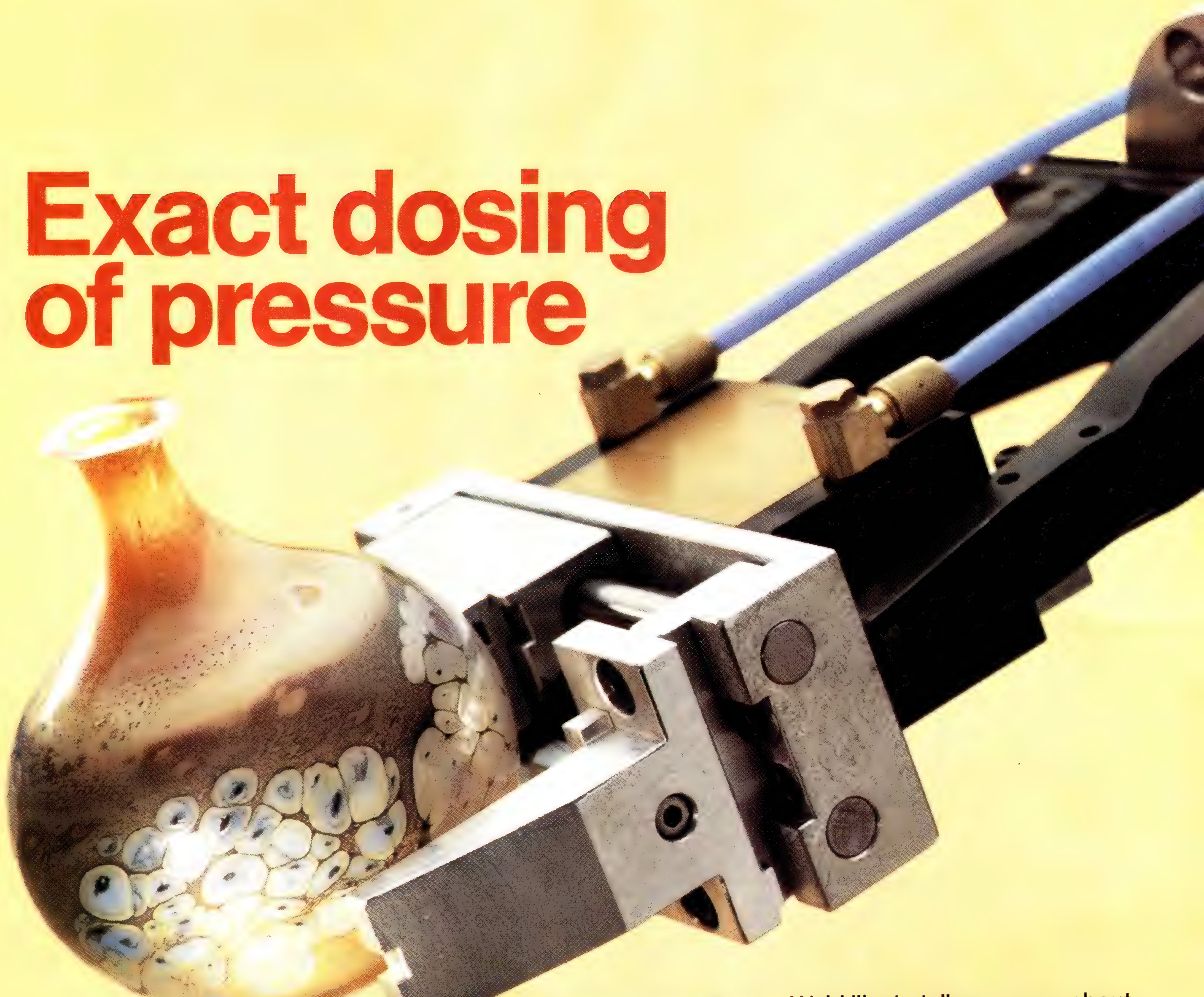
What the military has in mind is three levels of control over the publication of papers resulting from research it supports. The first level covers areas not considered sensitive and would require submission of papers to the department, for its information only, when they are submitted for publication. The second level concerns sensitive areas of basic research. Papers would be sent to the Pentagon 60 days before publication; its review would be advisory. The third level—the one that is causing all the trouble—would require submission 90 days before publication and give the Pentagon the right to insist on changes or to bar publication.

The Pentagon seems unwilling to understand two facts of technological life: first, without the cross-fertilization of free publication, the flow of advances would slow to a trickle; second, no matter how tightly the department restricts publication, it cannot build the perfect dam—take the atomic bomb as an example. It is also useful to note that in the Soviet Union, the exchange of ideas is severely restricted. What scientific or technological advance worth mentioning has come out of Moscow lately?

Gasing up the engines of science and technology

It's nice to see that even as the Pentagon tries to include more and more research and development in its embrace, the tempo continues to quicken. The University of Texas, moving smartly toward its avowed goal of becoming a world-class research institution to be mentioned in the same breath as the Caltechs, Stanfords, and MITs, has created 32 chairs, endowed for $1 million apiece, in the sciences and engineering. The money is coming from several sources. An anonymous Texan is giving $8 million, to be matched by five Texas foundations; the other $16 million will be contributed from a fund that traces its income to oil revenue.

The next time the gas pump races toward $30 or so for a fill-up, it will be comforting to realize that the ringing is really the sound of the boundaries of science and technology pushing outward in Austin.



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People

Signal processors will squeeze into one chip, says TI's French

As microprocessor markets have matured, semiconductor makers have tailored memory and central processors onto single chips to serve specific system applications. That fate could be in store for future generations of digital signal processors, suggests David D. French, who in March was named product manager for programmable communications chips at Texas Instruments Inc., in Houston.

Job-oriented. Texas Instruments' David D. French says application-specific signal processors could be in store down the line.

In his new post, the 27-year-old native of New York State will be responsible for TI's TMS320 digital-signal-processor family, modem chips, and speech line. The silicon-gate n-channel MOS TMS32010—a high-speed general-purpose signal processor that has been in production since the second half of 1983—is now being targeted at a wide range of duties. Selling for about $100 in 100-piece quantities, the chip, in plastic packages with the same 40-pin dual in-line configuration, will continue to come down in price.

Meanwhile, TI designers are putting the final touches on the next-generation 320 processor, reportedly set for introduction next year. Its data-path architecture will be enhanced for higher speeds with more parallel-processing capabilities along with more on-chip memory. But the chip will still be general-purpose.

French declines to discuss the future 320 product but does say that application-specific signal processors could emerge in the third generation. This might happen if the company tailors speeds and on-chip data streams with different architectures or makes additions to existing features, such as the 32010's current single-cycle 16-by-16-bit multiple instruction.

The first of TI's dedicated signal-processing peripheral chips—an analog input channel and an output channel (AIC/AOC)—were announced at the recent International Conference on Acoustics, Speech, and Signal Processing, in San Diego [*Electronics*, March 22, p. 42]. They are intended to ease the task of interfacing analog signals to and from 16-bit digital data buses, which could be controlled by a 320 processor.

"The third generation is still a little hazy. But as the industry and market for digital signal processing evolve, we will begin to have a clearer view of what types of customers will be served best with application-specific chips," says French, who joined TI in 1977, after completing his BSEE at the University of Rochester. Before his appointment to the communications product line, he was manager of TI's single-chip microcomputers.

Motorola's Morgan foresees memories with 'personality'

Semicustom memory chips? Well, not exactly. But as storage densities reach the megabit level, component makers will have to integrate the right "personality" into devices, says the new director of MOS memory marketing at Motorola Inc., in Austin, Texas.

"The market will definitely take on a new flavor in the megabit era," predicts Jack Morgan, 39, who served as Motorola's regional sales manager in Detroit before his recent move to central Texas. Morgan's past dealings with chip customers in the auto industry—many of them large-volume buyers of custom devices—will give him a feel for estab-

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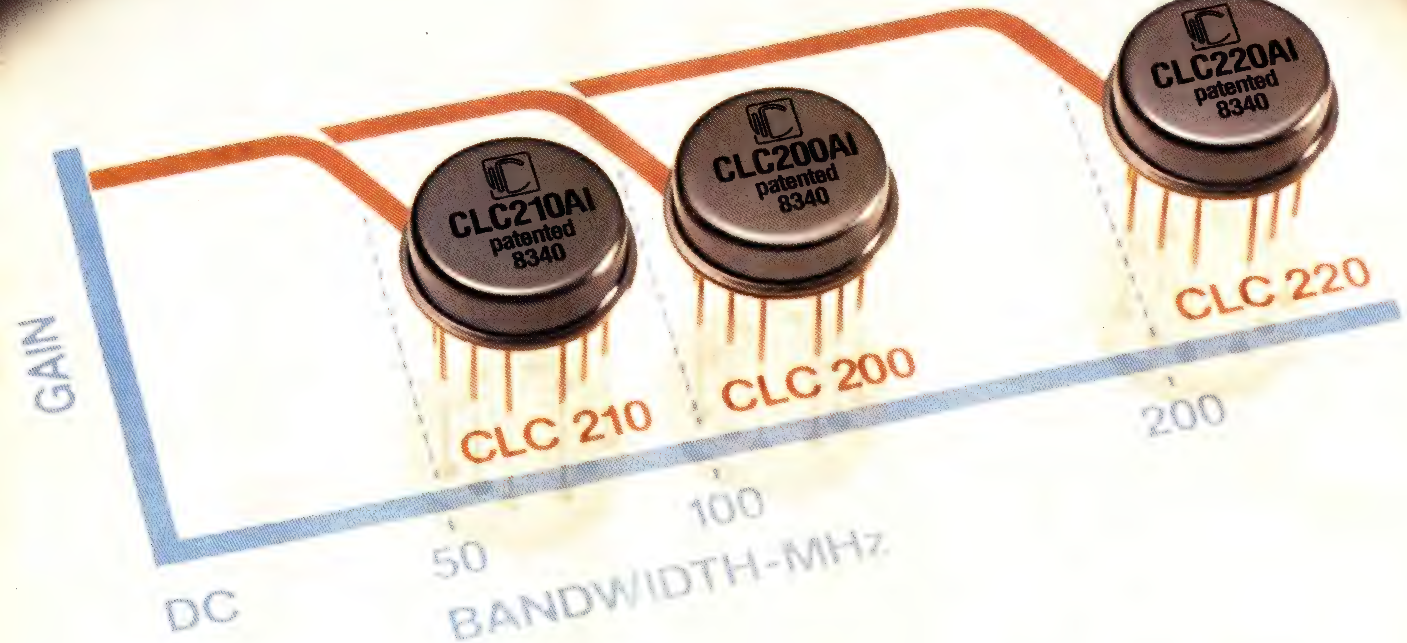

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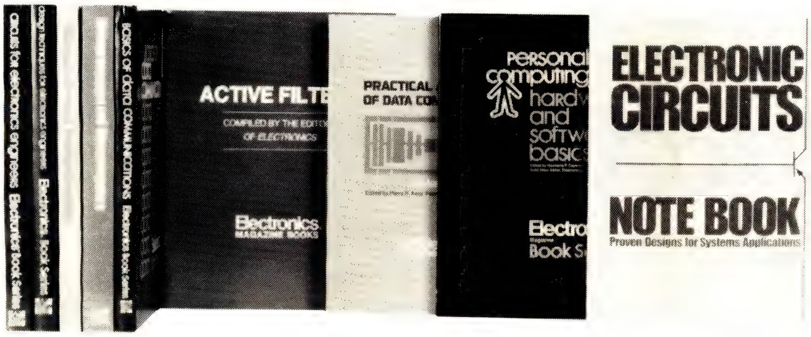
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People

Closer work. Jack Morgan of Motorola believes that larger memories will mean more application-specific designs.

lishing close ties with memory users.

"As memories get larger, much closer work [will be required] with the customer base," he notes, adding that Motorola already encourages "cross-pollination" between its field sales force and plant engineers. "No longer will the memory business be strictly a 'hunt' for universality; the search will be for the optimum and application-specific designs."

Megabit chips—and some at the 256-K level—are expected to have a wide range of features and on-chip logic. Winning the memory battles of the future will mean matching the right features to the right customer, believes Morgan, who joined Motorola as a product engineer in June 1967, after completing his BSEE at Arizona State University.

Nearly all Motorola's future MOS memories will have at least one common denominator: low-power complementary-MOS technology. Everything from 1-Mb dynamic random-access memories to erasable-programmable read-only memories will be made in C-MOS, he promises.

In addition, Motorola will continue to emphasize fast static RAMs, which the company regards as a key element in supporting future high-performance 16- and 32-bit microprocessors in its 68000 family. Morgan also believes that many RAM applications will favor statics over higher-density dynamic memories because fewer peripheral components are needed to support overhead. Such applications will include robotics, factory-automation equipment, and real-time computing systems.

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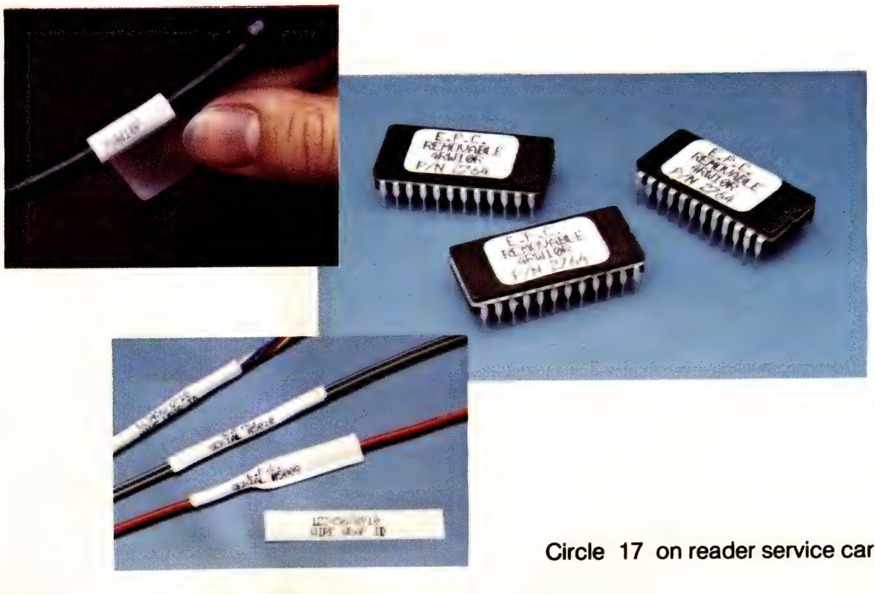

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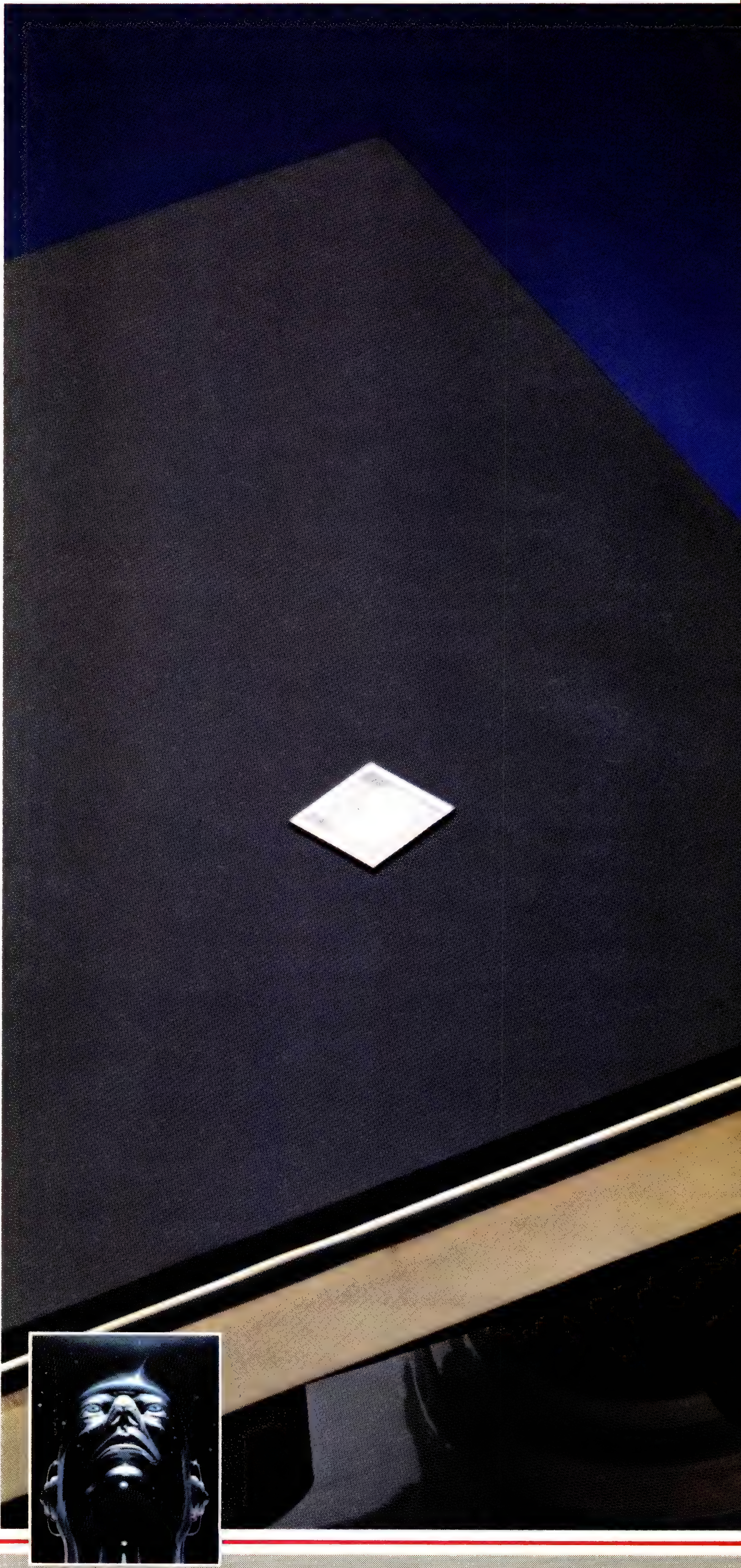

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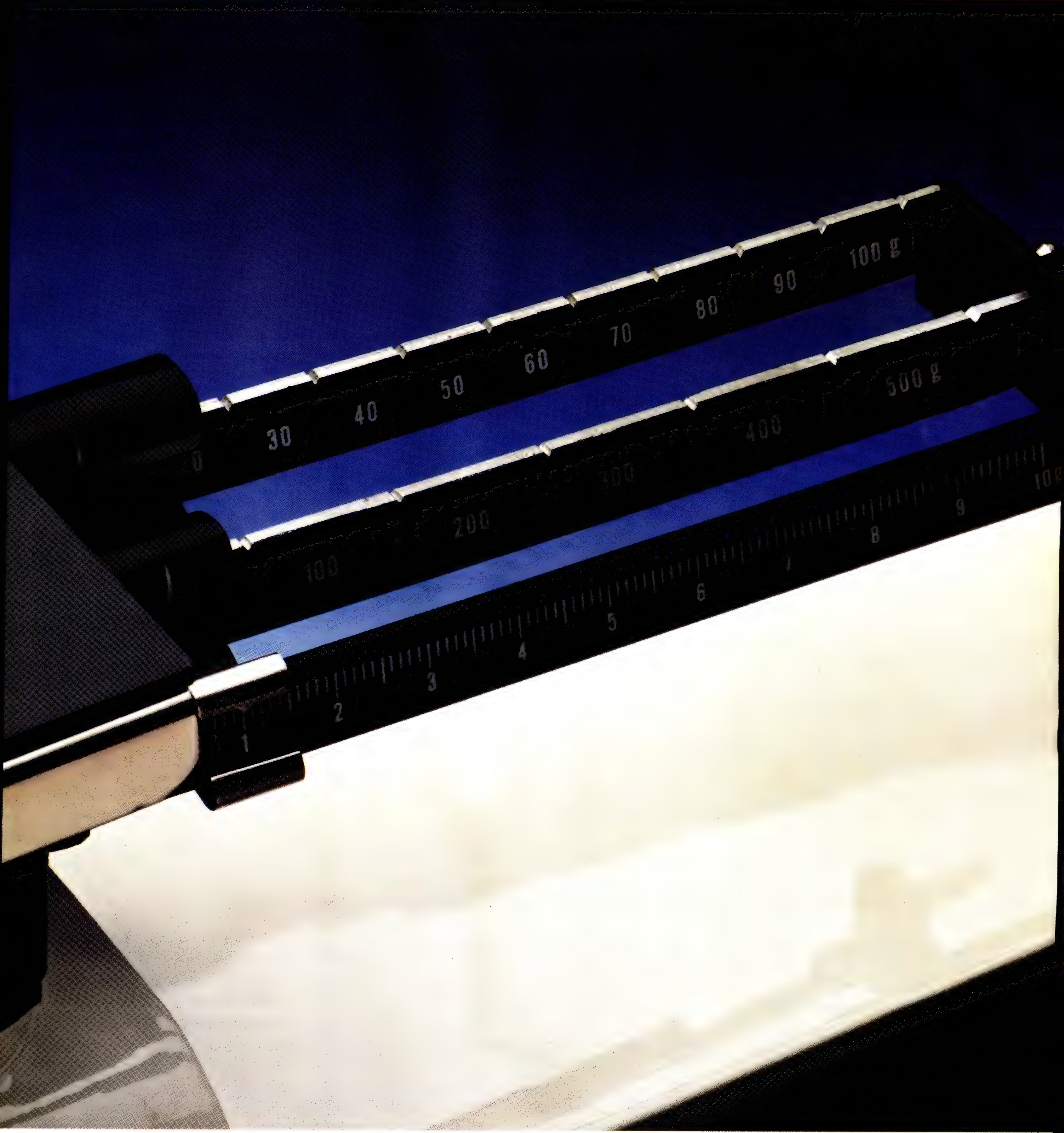

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In my opinion

It's time for a push on graphics standards

by Tom Clarkson
President, Graphic Software Systems

Twenty-odd months ago, Intel, Tektronix, and Digital Equipment Corp. (later joined by 12 other hardware and software manufacturers) announced plans for adoption of two computer-graphics standards: the Virtual Device Interface (VDI) and North American Presentation Level Protocol Syntax (NAPLPS). These companies hoped their alliance would spur the International Standards Organization and American National Standards Institute to quickly adopt graphics standards so that products incorporating them would begin appearing in the marketplace.

Nevertheless, progress has come slowly in deciding what standards are needed and in defining and adopting them. Technical complexity, vested interest on the part of manufacturers, and regional, national, and even international politics have thwarted adoption efforts.

Now we think another push can bring the graphics-standards effort to fruition. What's called for is some well-placed effort with the appropriate standards committees, coupled with timely introductions of hardware and software products incorporating draft versions of the major graphics standards. Such actions can help give the industry better graphics standards—and faster than we'll see them if major powers in the industry adopt a wait-and-see attitude and don't act until after the final standards have been adopted. The market needs standards badly: its potential can't be realized without them.

At present, NAPLPS, VDI, and the Graphical Kernal System (GKS) appear to have earned the support of the ISO and ANSI. The three are complementary: VDI and GKS are intrasystem standards, while NAPLPS is an intersystem standard.

VDI, a software standard, allows hardware-device independence. Graphics software based on VDI does not need to consider the characteristics of a specific output device but can deal with conceptual graphics models. GKS, a programmer's standard interface to define graphics functionalities, allows for easier incorporation of graphics into any application.

Transmitting graphics between systems requires a different standard—in this case, NAPLPS. It supports system-to-system communications and will accommodate higher-performance, higher-resolution hardware as it becomes available.

The problem the market faces at this point lies not in the standards themselves, but in the adoption process. By working with various standards organizations and industry groups, and incorporating the standards into products, computer-graphics equipment manufacturers can help both push and pull the standards into existence. Active involvement by the manufacturers will define the standards better and faster, and will also stimulate demand from the marketplace for products incorporating these standards. Once accustomed to graphics products that are portable and easier to use, the market will want more.

Some manufacturers are already taking such actions. Representatives of Intel, Graphic Software Systems, Hewlett-Packard, Tektronix, and other companies are serving on ANSI or ISO committees to help draft standards. Also, Intel is chairing a special-interest group that represents the manufacturers of graphics products within the National Computer Graphics Association.

Standards-based products, though difficult to design now because developers must anticipate what the standards will be, are already reaching the marketplace. At present, both VDI (as drivers) and GKS are being offered in some original-equipment-manufacturer software packages. As for hardware, VDI and NAPLPS products have already appeared in low-level-integration products as add-on graphics-only boards. The next-higher level, intelligent graphics subsystems, began appearing in 1982. The highest level of integration—entire standards-based graphics controllers on a chip—will likely appear sometime in 1985. (GKS, being much more complex, may not be entirely integrated into silicon.)

The manufacturers are not trying to sidestep the authority of the standards groups, merely giving the market what it is asking for. Following their lead by both building the standards into products now and actively supporting the standards organizations will help give us all better standards, faster.

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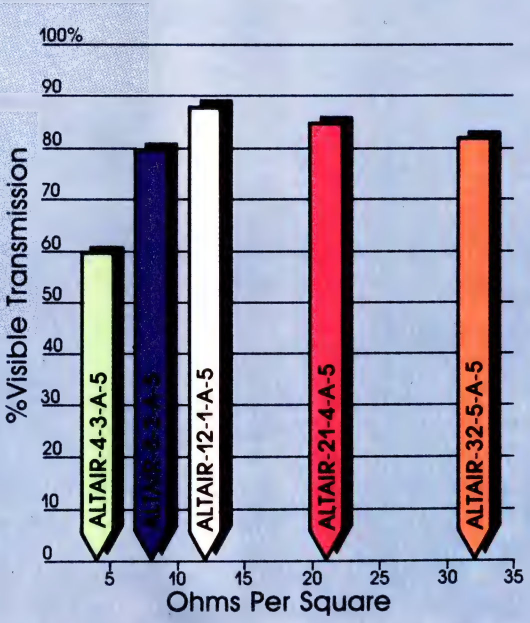

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Consumer Electronics Show, Electronics Industry Association (CES, 3 Illinois Center, Suite 945, 303 E. Wacker Dr., Chicago, Ill. 60601), McCormick Convention Center, Chicago, June 3–6.

International Symposium, Society for Information Display (Hilda Hammond, Palisades Institute, 201 Varick St., New York, N. Y. 10014), San Francisco Hilton, June 4–7.

Robots 8, Society of Manufacturing Engineers (RI/SME, Box 930, Dearborn, Mich. 48121), Cobo Hall, Detroit, June 4–7.

International Conference on Consumer Electronics, IEEE (Stuart J. Lipoff, Arthur D. Little Inc., 15 Acorn Park, Cambridge, Mass. 02140), Westin Hotel, Rosemont, Ill., June 6–8.

Ohmcon/84, IEEE (Electronic Conventions Inc., 8110 Airport Blvd., Los Angeles, Calif. 90045), Franklin County Veterans Memorial Auditorium, Columbus, Ohio, June 12–14.

Advanced Manufacturing Systems Exposition & Conference, Banner & Greif Ltd. (AMS 84, 708 Third Ave., New York, N. Y. 10017), McCormick Place, Chicago, June 12–14.

Summer 1984 Usenix Conference, Usenix Association and Software Tools Users Group Inc. (Usenix Conference Office, Box 385, Sunset Beach, Calif. 90742), Hotel Utah, Salt Lake City, June 12–15.

International Computer Show—Cologne, (Messe und Ausstellungs GmbH, Koln, Messeplatz Postfach 210760, D-5000 Koln 21), Cologne, Germany, June 14–17.

42nd Device Research Conference, IEEE (Pallab Chatterjee, Texas Instruments, M/S 369, Box 225621, Dallas, Texas, 75265), University of California, Santa Barbara, June 18–20.

13th International Conference on Quantum Electronics, American Physical Society, Optical Society of America, and IEEE (OSA, 1816 Jefferson Place, N. W., Washington, D. C. 20036), Anaheim Convention Center, Anaheim, Calif., June 18–21.

Conference on Lasers and Electro-Optics (CLEO), IEEE and Optical Society of America, (OSA, 1816 Jefferson Place, N. W., Washington, D. C. 20036), Anaheim Convention Center, Anaheim, Calif., June 19–22.

Armed Forces Communications and Electronics Association Conference and Exposition (AFCEA, 5641 Burke Center Parkway, Burke, Va. 22015), Washington Sheraton Hotel, Washington, D. C., June 19–21.

Computerized Office Equipment Expo/Office Information Systems Conference, Cahners Exposition Group (Janet Schafer, Cahners Plaza, P. O. Box 5060, Des Plaines, Ill. 60018), O'Hare Exposition Center, Rosemont, Ill. June 19–21.

First International Conference on Computers and Applications, IEEE (Harry Hayman, IEEE Computer Society, 1109 Spring St., Suite 300, Silver Spring, Md. 20910), Beijing (Peking), China, June 20–22.

26th Electronic Materials Conference, The Metallurgical Society of AIME (420 Commonwealth Drive, Warrendale, Pa. 15086), University of California, Santa Barbara, June 20–22.

IEEE VLSI **Multilevel Interconnection (V-MIC) Conference,** IEEE (Thomas E. Wade, Microelectronics Research Laboratory, Electrical Engineering Department, P. O. Drawer EE, Mississippi State University, State College, Miss. 39762), Hotel Inter-Continental, New Orleans, June 21–22.

Conference on the Forefronts of Large-Scale Computational Problems, American Federation of Information Processing, *et al* (Hal Raveche, A311 Physics Building, NBS, Washington, D. C. 20234), Gaithersburg, Md., June 25–27.

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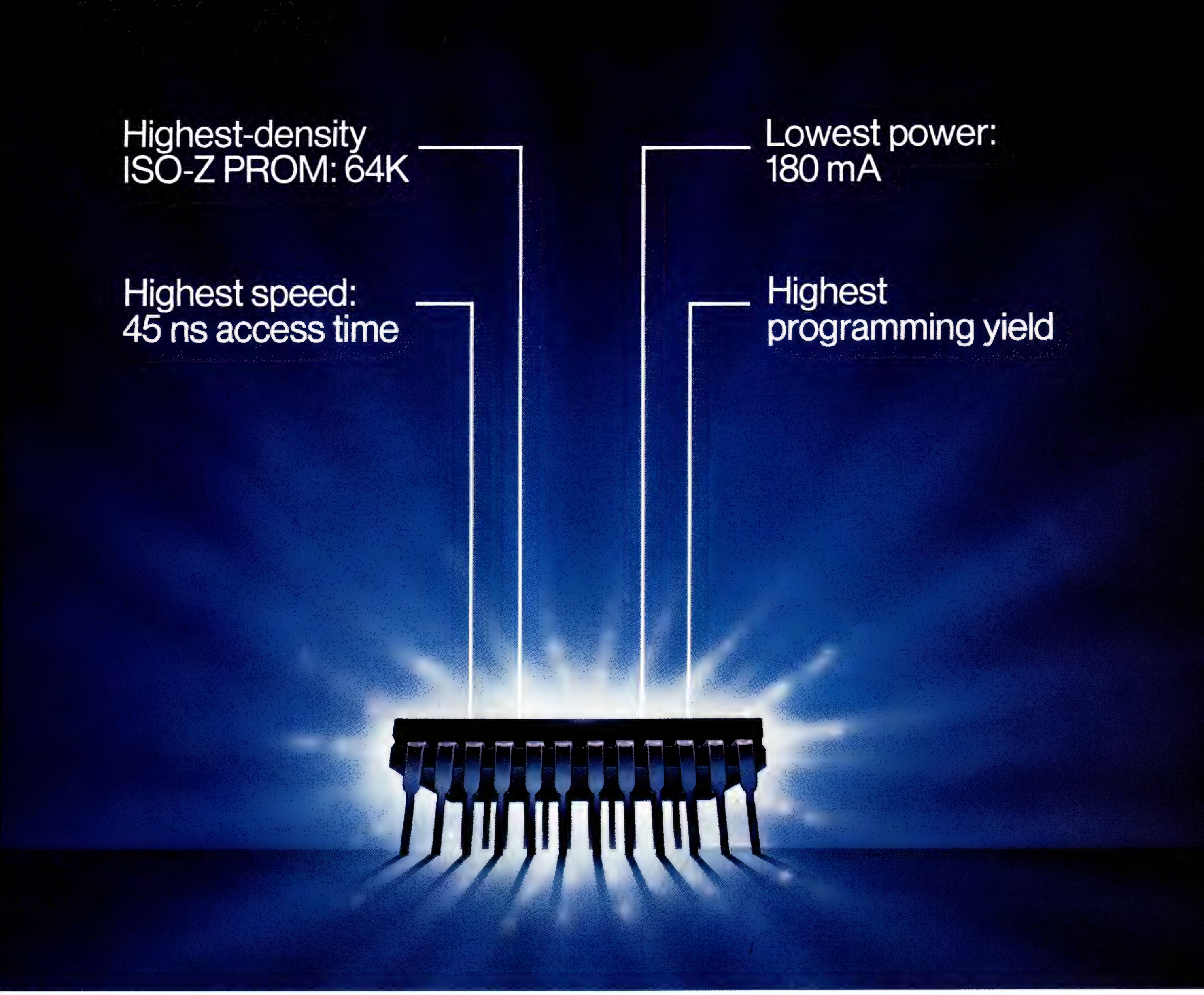
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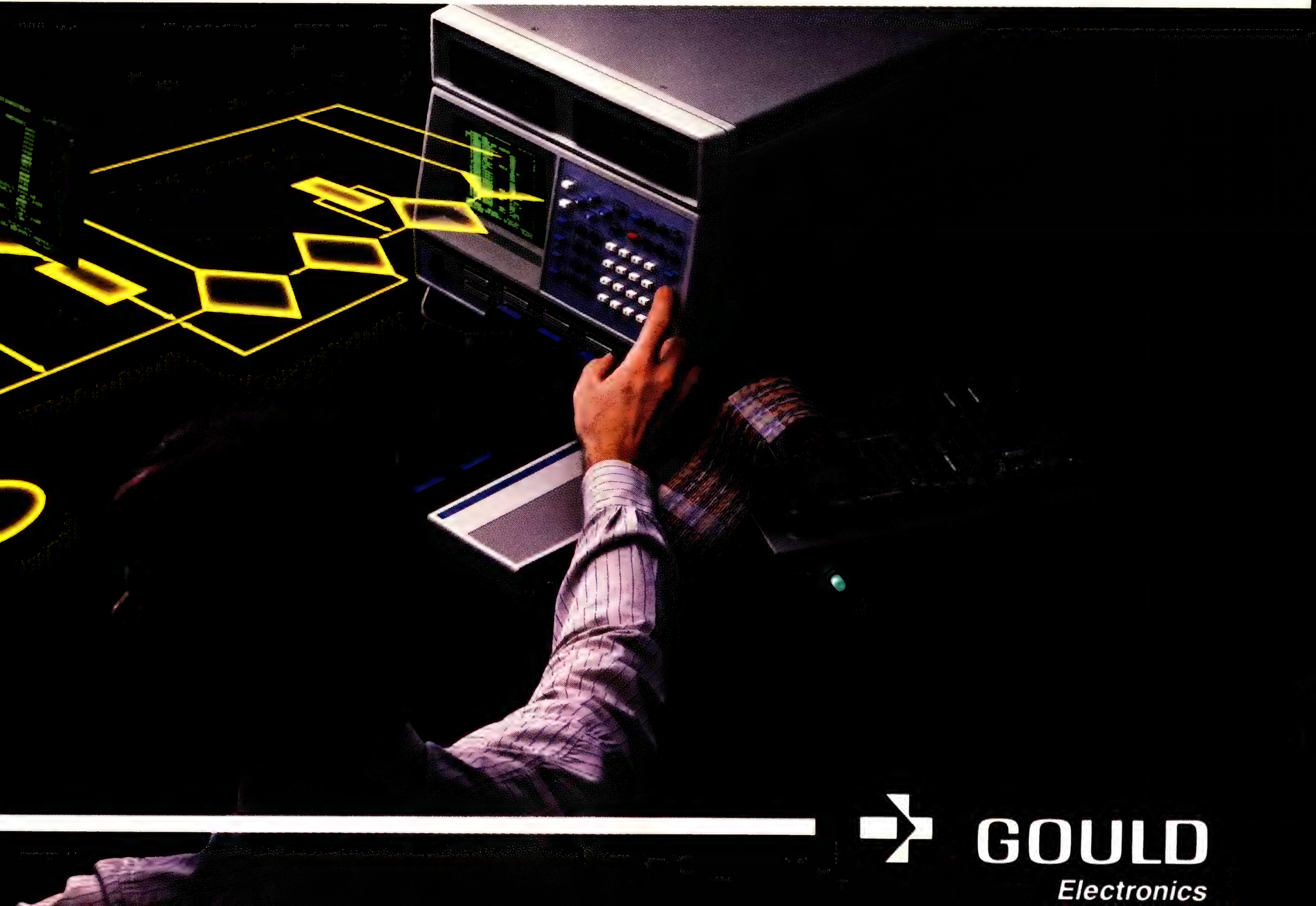

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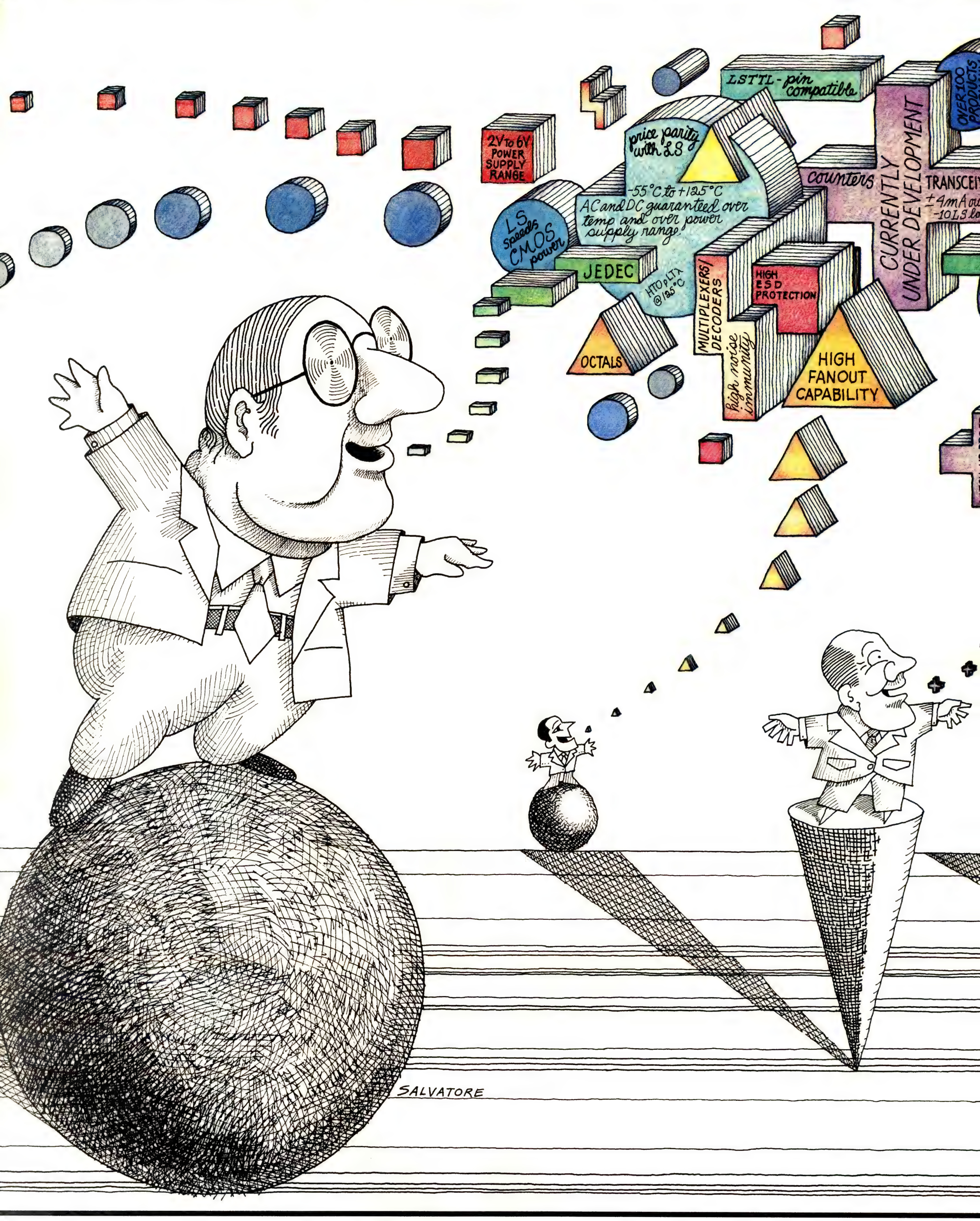2V to 6V POWER SUPPLY RANGE
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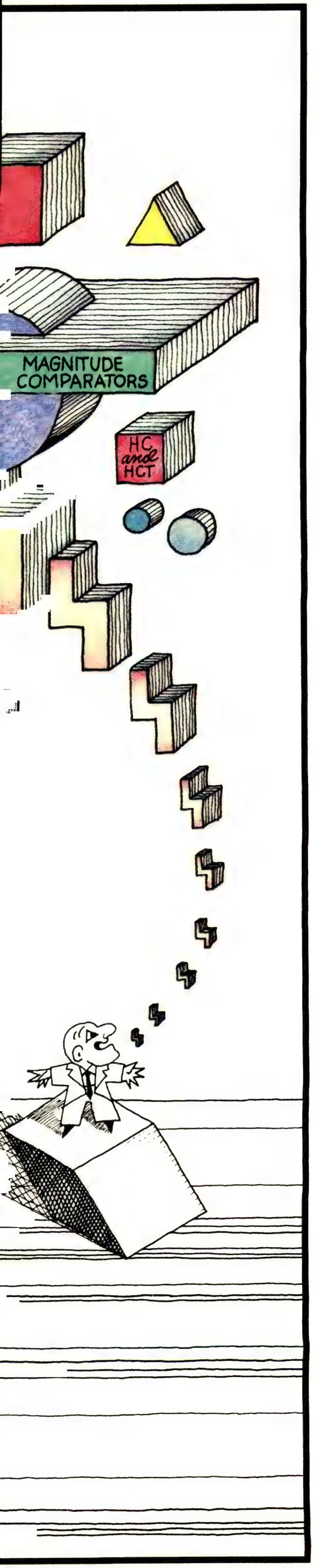

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News update

The future of Japan's controversial software bill remains in doubt. At a meeting in Honolulu on April 12–13, U. S. and Japanese government trade officials again failed to narrow their differences on a major point of dispute. The issue has delayed the drafting of software legislation that, in the words of one U. S. Commerce Department official, "will have international implications far beyond the U. S. and Japan" [*Electronics,* March 8, p. 105].

The key sticking point in the proposal, which is sponsored by the Ministry of International Trade and Industry—in Japan, legislation is generally drafted by the affected ministry rather than by individual legislators—is a provision that would allow a company to code and sublicense software, without the permission of the original developer.

Length of protection. Another disputed point is the MITI proposal that would limit software protection to 15 years. Software in most other nations is protected under copyright law for 50 to 75 years. Although such companies as International Business Machines Corp. and Burroughs Corp. still have software in operation that is as much as 25 years old, the point is less important to the U. S. side than it is to the Japanese.

MITI might still try to submit its measure to the current session of the Japanese Diet (parliament) but faces opposition not only from U. S. trade negotiators, who are acting at the urging of major U. S. computer manufacturers, but from the ruling Liberal Democratic Party. At the direction of Prime Minister Yasuhiro Nakasone, the LDP is trying to minimize U. S.-Japanese trade conflict, a goal that is not necessarily shared by the powerful government bureaucracy.

The LDP earlier had some success with this strategy when it forced a compromise involving certain aspects of the telecommunications law that had drawn foreign criticism for being too protectionist. Now, although Nakasone has not made a public statement concerning his position on the issue of software legislation, he might move to break the current deadlock as well. *–Michael Berger*

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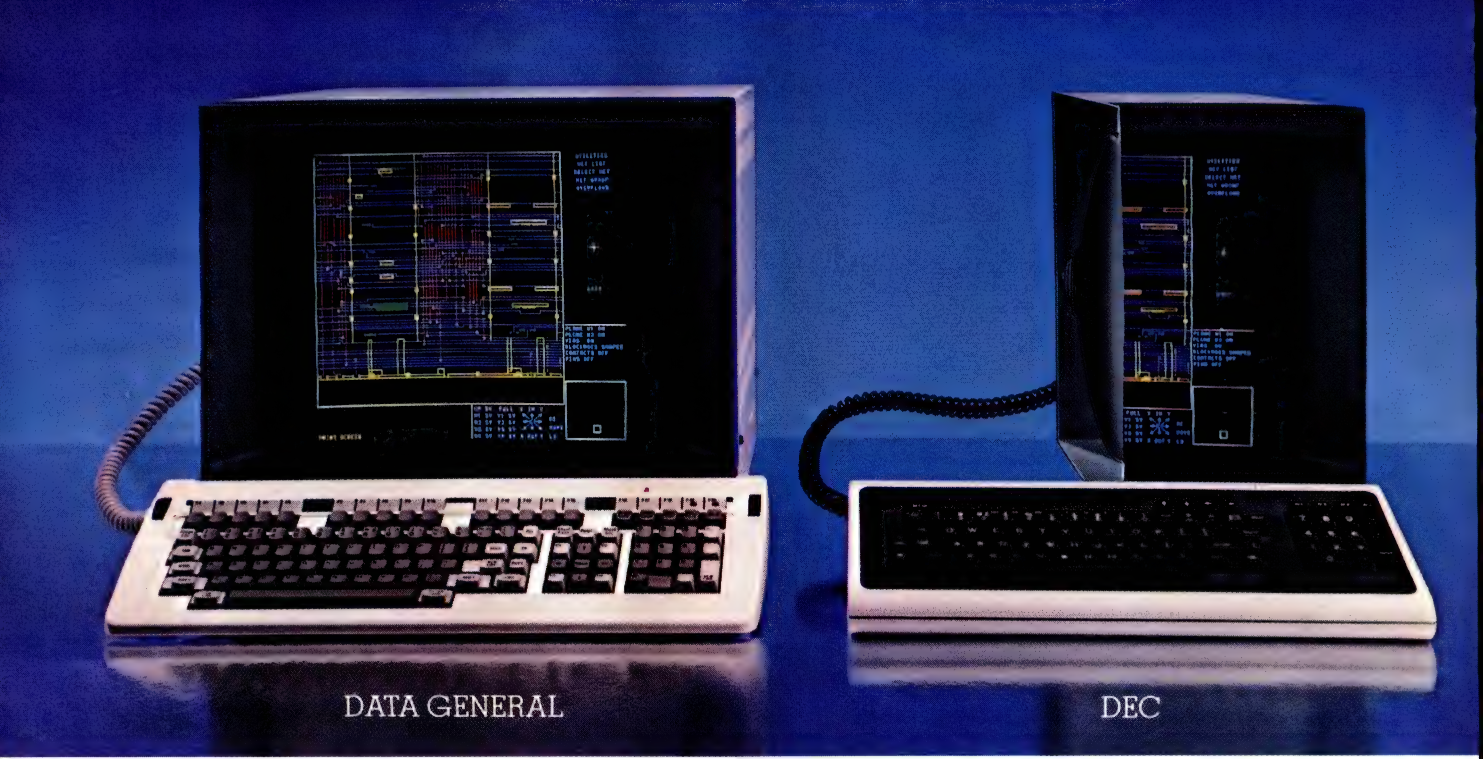

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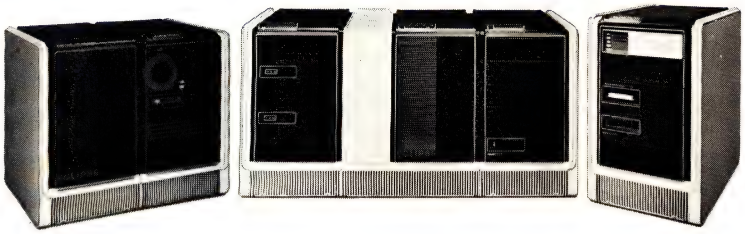

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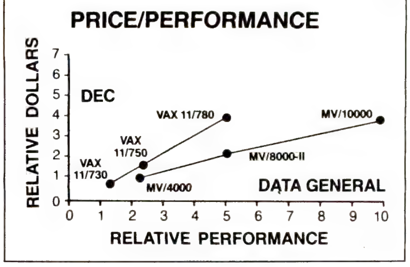

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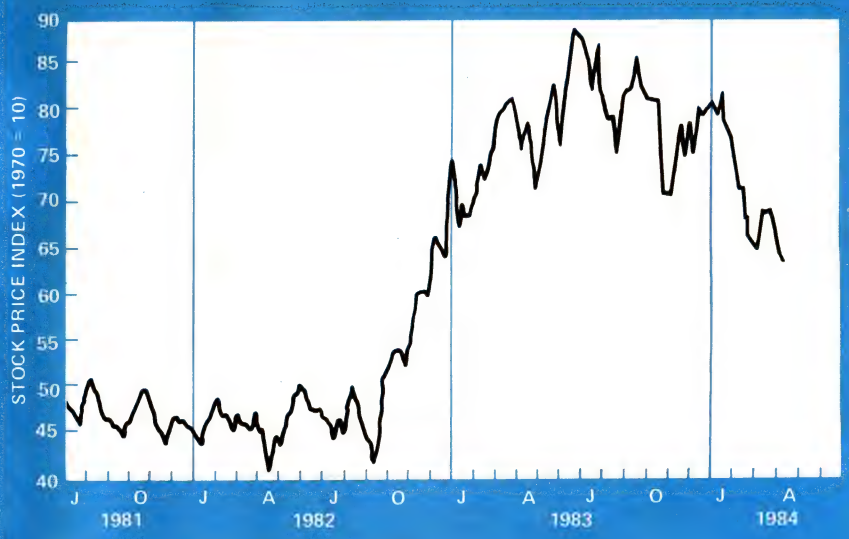


TRENDS IN INSTRUMENTATION STOCKS

SOURCE: STANDARD & POOR'S CORP

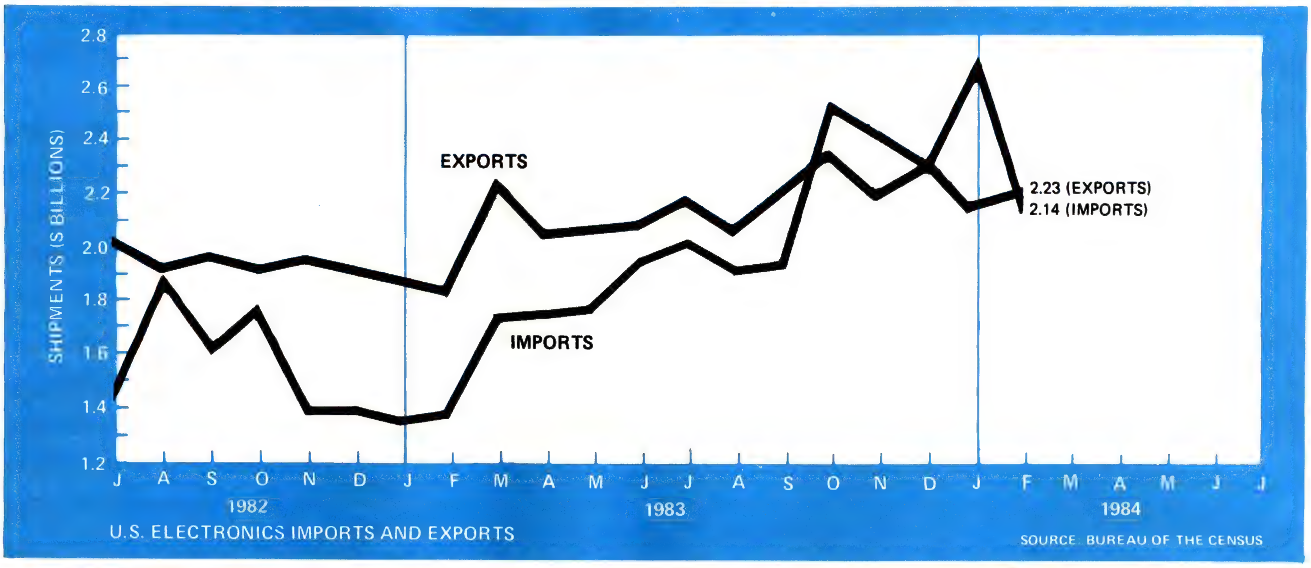
Sales of video-cassette recorders are continuing their torrid pace, according to the latest data collected by the Consumer Electronics Group of the Electronic Industries Association. VCR sales to retailers soared by 113% in March to 568,387 units from 266,501 units in the same month last year. For the entire first quarter, sales to retailers advanced almost 91% to 1,392,291 units from 729,565 in the 1983 first quarter, the EIA reports. Color-television-set sales to retailers in March showed good growth, increasing by over 25% to 1,553,618 units from 1,238,027 units a year ago. For the first quarter, color TV sales to retailers are up 26% to 3,838,359 units versus 3,042,478 last year. Black and white TV-set sales continue to decline, by 18% in March to 443,860 units from 544,877 a year ago, and by 10% in the first quarter, to 1,173,370 units from 1,310,737 in 1983.

With sales of VCRs continuing to be strong, sales to retailers of color video cameras increased strongly in March as well, gaining 41% to 37,445 units versus March 1983 sales of 26,497 units. For the first three months of this year, camera sales rose 32% to 98,209 units compared with sales of 74,418 units in the first three months of 1983. In projection TV sets, the EIA's Consumer Electronics Group reports that sales to retailers in March were up 28% to 13,969 units, compared with the 10,896 units sold in the same month a year ago. Sales of projection TVs for the 1984 first quarter advanced 20% to 38,536 units from 31,981 units in the same 1983 period. The Consumer Electronics Group notes that its data "reflects total market statistics for products produced and/or sold in the U.S., regardless of the brand name or country of origin."

Company financings... *Plexus Computers Inc.,* Santa Clara, Calif., maker of a Unix-based supermicrocomputer system, raised $6.4 million in new financing.... *Electronic Systems Products Inc.,* Titusville, Fla., completed a $3 million equity financing. The firm makes computer video projectors for computer graphics and teleconferencing applications.... A total of $5.5 million will flow into the coffers of vision inspection system maker *Machine Vision International,* Ann Arbor, Mich., under terms of an agreement signed with a group of investors. The group includes Safeguard Scientifics Inc., a technology management firm in King of Prussia, Pa.... *Saber Technology Corp.,* San Jose, Calif., received $1 million in new financing to fund its work on an interactive graphics work station for automated design.

–Robert J. Kozma

Business activity



U.S. ELECTRONICS IMPORTS AND EXPORTS

SOURCE: BUREAU OF THE CENSUS

U.S. ELECTRONICS IMPORTS AND EXPORTS[1] (MILLIONS OF DOLLARS)

	IMPORTS			EXPORTS		
	Feb. 1984	Jan. 1984	Feb. 1983	Feb. 1984	Jan. 1984	Feb. 1983
Accounting, computing, and data-processing machines	208.577	309.191	88.574	492.703	475.273	413.259
Calculators	32.141	63.434	34.500	7.555	8.685	6.140
Parts for data-processing machines and office calculators	268.404	372.092	157.800	489.063	414.473	352.224
Telecommunications, sound-recording, and sound-reproducing equipment	1,023.293	1,209.557	683.163	287.958	360.602	269.831
Electronic or electric instruments	90.711	123.238	66.660	464.978	458.558	455.959
Printed-circuit boards	15.666	18.830	15.749	18.390	18.131	10.791
Integrated circuits, diodes and other semiconductors, tubes, piezoelectric crystals, parts	483.509	597.937	332.977	458.817	418.289	326.340
Fixed and variable resistors	22.542	25.100	13.059	14.639	15.356	10.073

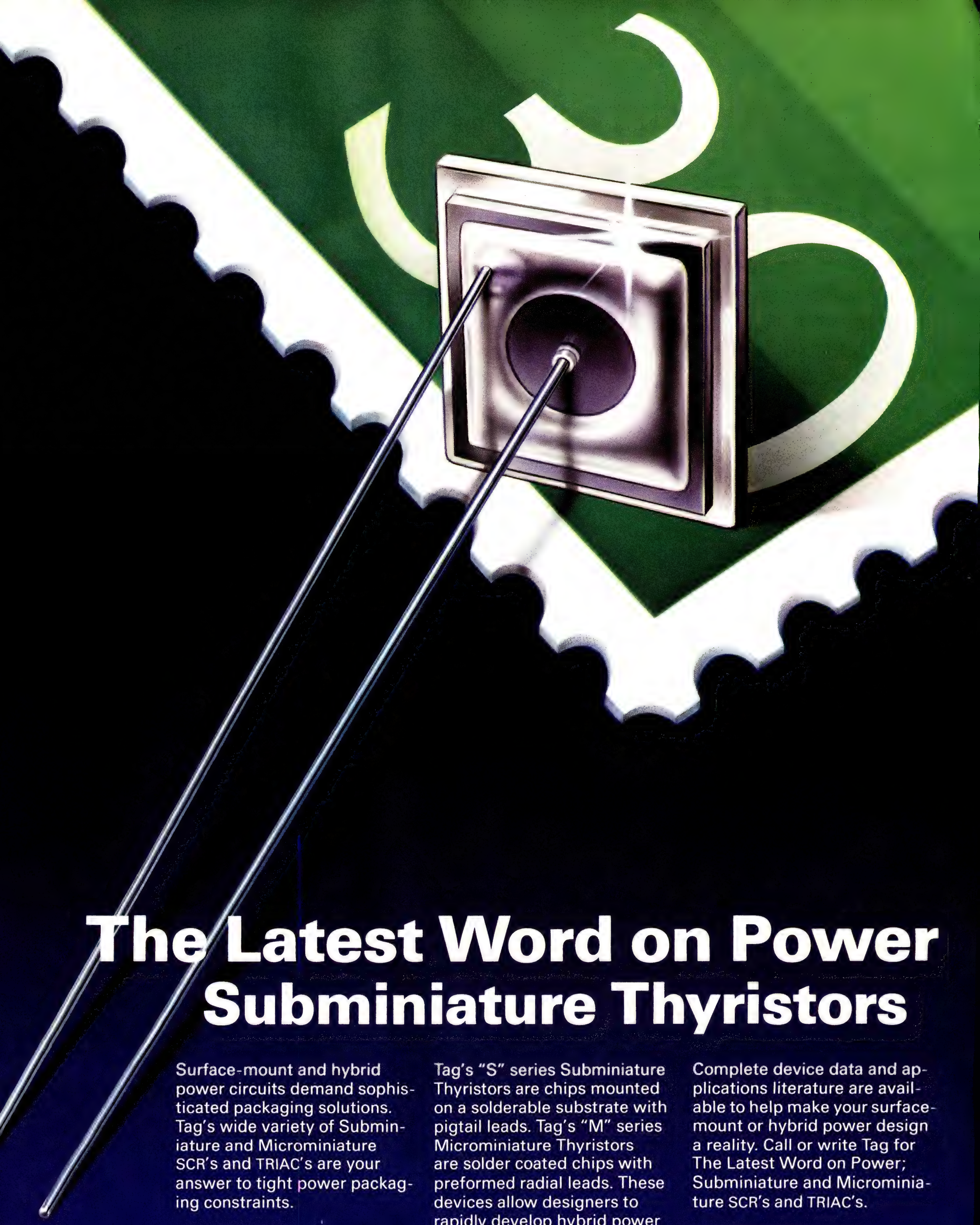
U.S. ELECTRONIC-COMPONENTS PRODUCER PRICE INDEX[2] (1967 = 100)

	February 1984	January 1984	February 1983
Digital bipolar integrated circuits	64.0	64.0	48.8
Digital MOS ICs	40.6	42.5	40.5
Linear ICs	64.7	63.7	60.7
Capacitors	191.5	191.6	190.5
Resistors	186.4	185.5	183.1
Relays	301.3	301.3	232.0
Connectors	226.1	225.2	222.6

GENERAL U.S. ECONOMIC INDICATORS

	March 1984	February 1984	March 1983
Average prime rate (%)[3]	11.21	11.00	10.50
Retail sales ($ billions)[4]	103.400	105.744	93.804
Unemployment rate (%)[2]	7.7	7.7	10.2

SOURCES: [1] Bureau of the Census [2] Bureau of Labor Statistics [3] Federal Reserve Board [4] U.S. Department of Commerce



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Circle 37 on reader service card

The importance of getting the most out of the investments you make.

This man isn't getting the most from his umbrella investment. GenRad believes many electronics manufacturers aren't getting the most from their ATE investment. We can show you how your ATE can dramatically improve the quality of your products.

Many times, companies faced with problems have the solutions to those problems close at hand.

This can be especially true for many electronics manufacturers.

These companies are faced with the problem of improving the quality of their products. And improving productivity and profitability.

And like the man above, these companies have the solutions to their problem close at hand.

The solution is their automatic test equipment (ATE) and how they make the best use of it.

GenRad can show you how to solve the problem of improving the quality of your products. By showing you how to get the most from your ATE investment.

We call this concept Quality Management.

Why ATE is such an important investment.

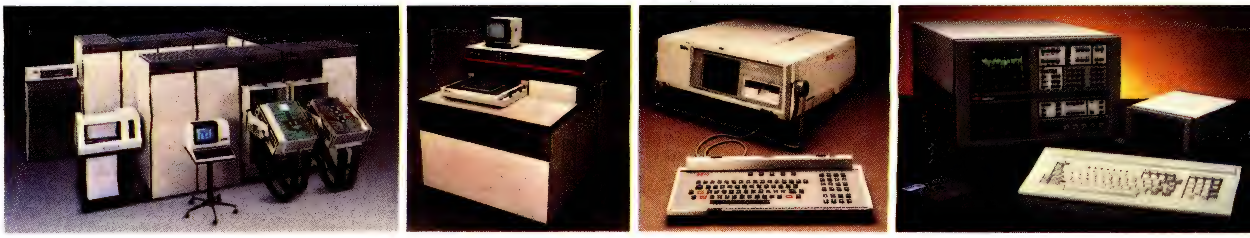
Chances are, you're already using ATE.

To test components, subassemblies and finished assemblies.

Your ATE helps you find out what's good and what's bad. If it's bad, you weed it out or repair it.

But this method is simply *measuring*

GenRad offers the broadest line of testers in the industry. We offer systems spanning the total Engineering/Manufacturing/Service process.



quality. Finding defects after they've already occurred.

Today, measuring quality isn't enough. You must learn to *manage* quality.

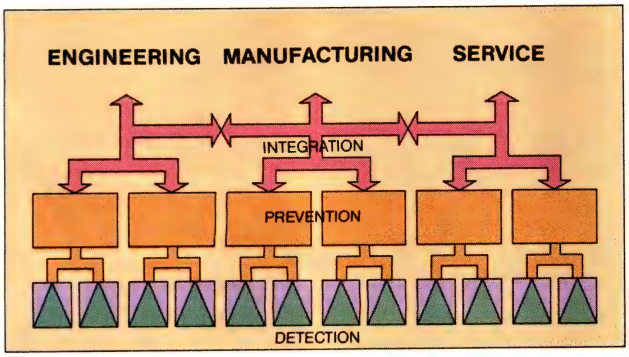
When you manage quality, you can improve the *process* that creates your products.

You can *prevent* faults instead of just finding them.

But first, you must learn how to leverage your ATE investment.

How to leverage your ATE investment.

Any systematic approach to Quality Management must start with the data created by ATE.



There are three levels of Quality Management. Level 1 is fault detection. Level 2 is fault prevention. Level 3 is the integration of quality information throughout the entire process. As you can see, Quality Management builds up from a solid base of testing capability.

There's simply no place else to get it.

But that data by itself won't help you improve quality. Unless you *leverage* it.

To leverage, you must apply powerful Quality Management Software to sort reams and reams of test data. And extract meaningful quality information.

Then you must put that quality information to use where it can do you the most good.

When you leverage, you'll be able to identify trends. You'll be alerted to emergency situations. And you'll be able to monitor the extent of improvements in quality. Automatically and in real-time.

As a result, you'll be able to actually manage and improve quality. And you'll get a better return on your ATE investment.

The solution is at hand today.

Quality Management is not some futuristic notion.

But to make Quality Management work, you do need three things.

First, you need ATE. And GenRad offers the broadest line of ATE in the industry.

Secondly, you need to learn to leverage. Again, GenRad offers the tools you need, hardware and software, that can help you move to higher levels of quality.

Already, several of our Quality Management products are helping customers realize significant improvements in quality.

Products like TRACS™ – a system that helps you lower costs, reduce in-process inventories, and dramatically increase the capacity of your production test and repair process.

And SCAN™ – a system that helps you improve the quality of incoming components and the productivity of your incoming inspection process.

Finally, you need a company that's willing to work with you in solving your special problems. GenRad provides more of that kind of custom applications support than anyone in the industry.

GenRad's approach to Quality Management.

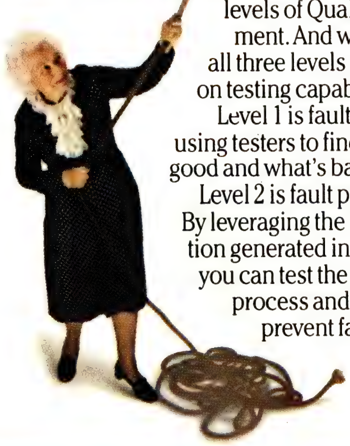
At GenRad, we believe there are three levels of Quality Management. And we believe all three levels depend on testing capability.

Level 1 is fault detection – using testers to find out what's good and what's bad.

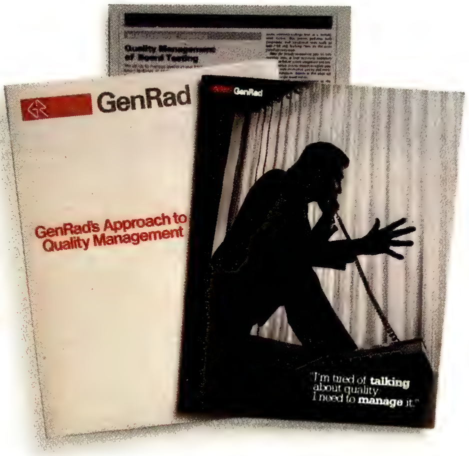
Level 2 is fault prevention. By leveraging the information generated in Level 1, you can test the entire process and fix it. You prevent faults instead of just finding them.

Level 3 is the integration of Quality Management – where quality information is disseminated throughout the engineering, manufacturing and service process, and up to your broader purpose business control system.

GenRad offers products at all 3 levels.



When you use leverage, you can perform tasks that would be otherwise impossible. GenRad can show you how leveraging your ATE investment can dramatically improve quality.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For more information about GenRad's approach to Quality Management, call 1-800-621-6260 or write us at: GenRad Inc., MS/654, 170 Tracer Lane, Waltham, MA 02254.

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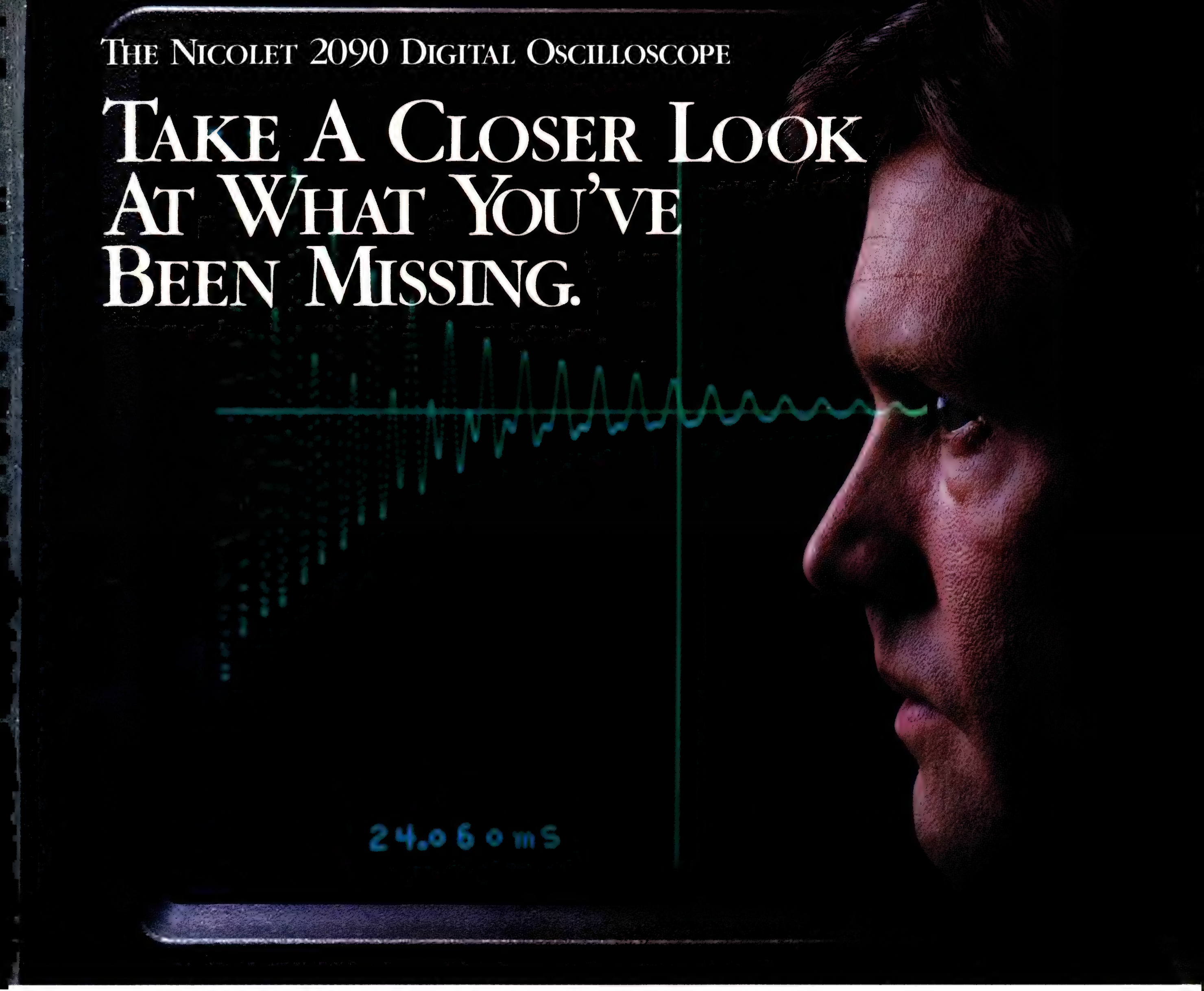

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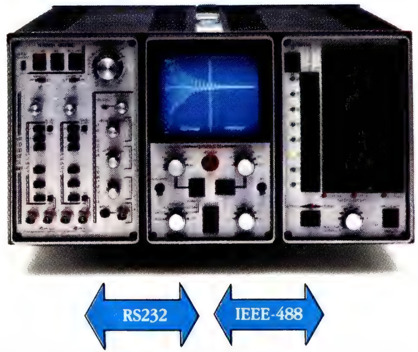
DON'T MISS ANY TRANSIENTS.

The 2090 offers push button transient capture, at speeds selectable from 20 nanoseconds to 200 seconds per point, so you can record fast or slowly changing signals with ease. And *pre- and post-trigger capture* lets you see what led up to an event as well as what followed. Built-in floppy disk allows unattended operation . . . just set and forget.

THE VERSATILITY YOU'VE BEEN LOOKING FOR.

Optional RS232 and IEEE-488 bidirectional interfaces give you the ability to coordinate and manipulate data by remote computer. That means the 2090 scope can be the front end of an entire analysis system. Not only that, the 2090's modular design allows you a choice of *four different plug-ins.* Pick the digitizer that's designed for your present application, and add other plug-ins to fit your expanding needs in the future.



SEE FOR YOURSELF.

Let us show you how easy the 2090 is to use. It's time *you* started benefiting from the tremendous digital advantage. Call us: **(608) 273-5008.** Or write: Nicolet Oscilloscope Division, 5225 Verona Road, Madison, WI 53711.

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Electronics newsletter

Apple attacks IBM in the home market with new IIc, price cut

With the avowed intention of taking a bite out of IBM's PCjr home computer business, which IBM says hasn't met expectations, Apple Computer Inc. has with much hoopla unveiled a 7.5-lb. portable—the Apple IIc—selling for $1,295. A comparably equipped PCjr costs $1,269. At the same time, **Apple cut the price of its IIe from about $1,800 to $995.** Labeled a serious computer for the home, the IIc is based on the architecture of the IIe and has a 65C02 processor. It can run about 90% of the more than 10,000 programs already available for the Apple II family. The new computer comes complete with 128-K of random-access memory, a half-height 5¼-in. disk drive, a 63-key keyboard, and ports for an external disk drive, video monitors, a mouse or game controller, and dc power, as well as two serial ports—all in an 11.5-by-12-by-2.5-in. package. The unit also has a built-in 5-octave synthesizer, can switch between 40- and 80-column text display, and can be used with a color or an ultrahigh-resolution (560-by-192-picture-element) monochrome display. A flat-panel display should be available this fall for about $600.

Motorola lines up Toshiba to build its a-m stereo IC

Late last month, Motorola Inc. fired another salvo in the battle of competing a-m stereo systems: a joint announcement with Toshiba Corp. to the effect that Toshiba will second-source Motorola's C-QUAM a-m stereo decoder IC. The deal should ease the concerns of Japanese receiver manufacturers, who "are a little uncomfortable if they have to source any of their IC requirements in the U. S.," says Oscar Kusisto, a special a-m stereo consultant for Motorola. In addition, **the agreement may help win over receiver manufacturers who have refrained from endorsing the Motorola stereo decoder as a result of concerns about chip availability,** Kusisto says. A case in point is Pioneer Electronic Corp., which was expected to announce plans to build single-system receivers using the Motorola system. (Single-system receivers are compatible with only one of the four competing broadcast schemes, from Motorola, Kahn Communications, Harris, and Magnavox.)

Supermini to offer supercomputer muscle

A Minneapolis start-up known as Edge Computer Corp. plans to produce a superminicomputer aimed at the scientific and engineering market. **The supermini is said to provide supercomputer-class performance for an individual user at a fraction of a supercomputer's price.** The firm, says president Alex Cimochowski, will use complementary-MOS technology licensed from Control Data Corp. He will provide few other details on the product, which is set for first shipments in next year's first quarter. Following a $1.1 million round of seed funding last fall, the firm went on to obtain an additional $10 million in financing in March.

Supercomputer speeds for under $1 million

A synchronized parallel processor that achieves supercomputer performance in the matrix operations it was designed for will be available this year from Floating Point Systems Inc., of Portland, Ore. The new 164 MAX will perform 124 parallel adds or multiplies and achieves a performance of 33 million to 341 million floating-point operations/s—the range depends on the amount of replication in the matrix operations.

Electronics newsletter

A fully configured version will cost less than $1 million, Floating Point says. Supercomputers delivering the same range of floating-point operations—although with greater general arithmetic capability—cost well over $10 million. **The unique MAX architecture has a single independent processor,** which performs parallel operations by writing vectors to arithmetic cells mapped into the top megaword of its 16 million words of 64-bit memory. Custom floating-point processors determine the arithmetic function, so that as the second vector is written, the product is automatically computed. The computer is built with standard Schottky logic and 200-ns 64-K memory chips.

Compass offered as military portable

Spotting a potentially major military and aerospace market for rugged portable computers—though one that is becoming increasingly competitive—SAI Technology Co., of San Diego, Calif., has joined with GRiD Systems Corp., of Mountain View, Calif., to ruggedize and produce a militarized version of GRiD's Compass system by year end. **The 10-lb package measures 15 by 11.5 by 2 in.—the size of a small attaché case—** uses an Intel 8086 16-bit microprocessor plus an Intel 8087 80-bit high-speed arithmetic coprocessor, and has 256-K bytes of random-access memory, 384-K bytes of nonvolatile bubble memory, and 16-K bytes of read-only memory. The display is a 6-in. electroluminescent amber model. First priced at $20,000 to $100,000—compared with $6,000 to $12,000 for commercial Compass units—the GRiDSET will join entries from Litton Industries, Magnavox, and Singer.

Mostek splits system and semiconductor units

To reduce its dependence on recession-sensitive sales of dynamic random-access memories still further, Mostek Corp., of Carrollton, Texas, has reorganized to stimulate product diversification, both in chip and computer-system markets. With that goal in mind, **the United Technologies Corp. subsidiary has established independent Semiconductor and Systems Technology operations, under two vice presidents.** Heading the reorganized semiconductor activity will be Robert B. Palmer, promoted to executive vice president of the corporation. John W. McNeley, vice president and general manager, will head the systems efforts. Both report directly to Mostek president Harold Ergott Jr.

Addenda

International Business Machines Corp. has developed an experimental megabit random-access memory, the first of its size by a U. S. company. Several Japanese companies also have developed 1-Mb devices but have not yet marketed them. The largest commercially available chip is AT&T's 256-K RAM. **IBM will not say when its megabit chip will be ready for commercial use.** . . . The copy-cat business continues to be profitable for Compaq Computer Corp., in Houston, maker of IBM-compatible computers. **Compaq reports first-quarter sales of $62.9 million and earnings of $3.3 million,** or 12¢ a share. In the first quarter of 1983, sales were $4.9 million, for a net loss of $3.2 million. . . . AT&T Information Systems, Morristown, N. J., has unveiled **the System 75 integrated business-communications system, which offers IBM terminal emulation as an option.** It permits AT&T's models 500 and 515 terminals to act as IBM 3270 or 2780/3780 asynchronous terminals over regular phone lines within a building.

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Hex Inverter

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Triple 3-Input AND Gate

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Dual One-of-Four Decoder/ Demultiplexer

8-Bit Priority Encoder

8-Input Multiplexer

Dual 4-Input Multiplexer

Quad 2-Input Multiplexer

Up/Down Decade Counter

Up/Down Binary Counter

Hex D Flip-Flop w/Common Master Reset

Quad D Flip-Flop w/Common Master Reset

Arithmetic Logic Unit*

Carry Lookahead Generator

64-Bit Memory

Octal Inverting Bus/Line Driver

Octal Bus/Line Driver

Quad Bus Transceiver

Octal Bus/Line Driver

Octal Bus Transceiver

Octal Shift/Storage Register

Octal Shift/Storage Register

Octal Shift/Storage Register

4-Bit Shifter

Dual 4-Input Multiplexer

Dual 4-Input Multiplexer

Binary Serial/Parallel Multiplier 8 x 1

Quad Serial Adder/ Subtractor

4-Bit Flip-Flop True & Complement Outputs

4-Bit Flip-Flop True Output

Multimode Octal Latch*

Inverting Multimode Octal Latch*

Dual One-of-Four Decoder

Octal Bus Transceiver

3-Line to 8-Line Decoder, Latched Inputs

3-Line to 8-Line Decoder

4-Bit Decade Counter

4-Bit Binary Counter

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4-2-3-2 Input AND-NOR Gate

Dual D-Type Flip-Flop

Quad 2-Input Exclusive-OR Gate

Dual J$\overline{K}$ Flip-Flop

Quad 2-Input Multiplexer

BCD Decade Counter Asyn. Reset

4-Bit Binary Counter Asyn. Reset

BCD Decade Counter Synch. Reset

4-Bit Binary Counter Synch. Reset

Serial-In/ Parallel-Out Shift Register

64-Bit Memory

Up/Down Decade Counter

Up/Down Binary Counter

Up/Down Decade Counter

Up/Down Binary Counter

4-Bit Bidirectional Universal Shift Register

8-Input Multiplexer

Dual 4-Input Multiplexer

Quad 2-Input Multiplexer

Quad 2-Input Multiplexer

9-Bit Parity Generator/ Checker

4-Bit Full Adder

Octal D Flip-Flop

Octal D Flip-Flop

Hex D Flip-Flop with Enable

Quad D Flip-Flop with Enable

Arithmetic Logic Unit

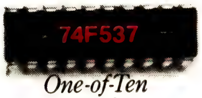
Arithmetic Logic Unit

Octal Comparator

8-Bit Register Comparator

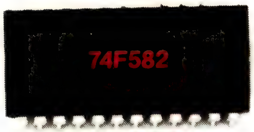
Inverting Octal D Latch

Inverting Octal D Flip-Flop



One-of-Ten Decoder

One-of-Eight Decoder



4-Bit BCD Arithmetic Logic Unit

4-Bit BCD Adder

GPIB Compatible Octal Transceiver

*16-Bit Serial-In/ Serial-Parallel-Out Shift Register**

*16-Bit Serial-Parallel-In/ Serial-Out Shift Register**

8-Bit Serial Multiplier with Adder/ Subtractor

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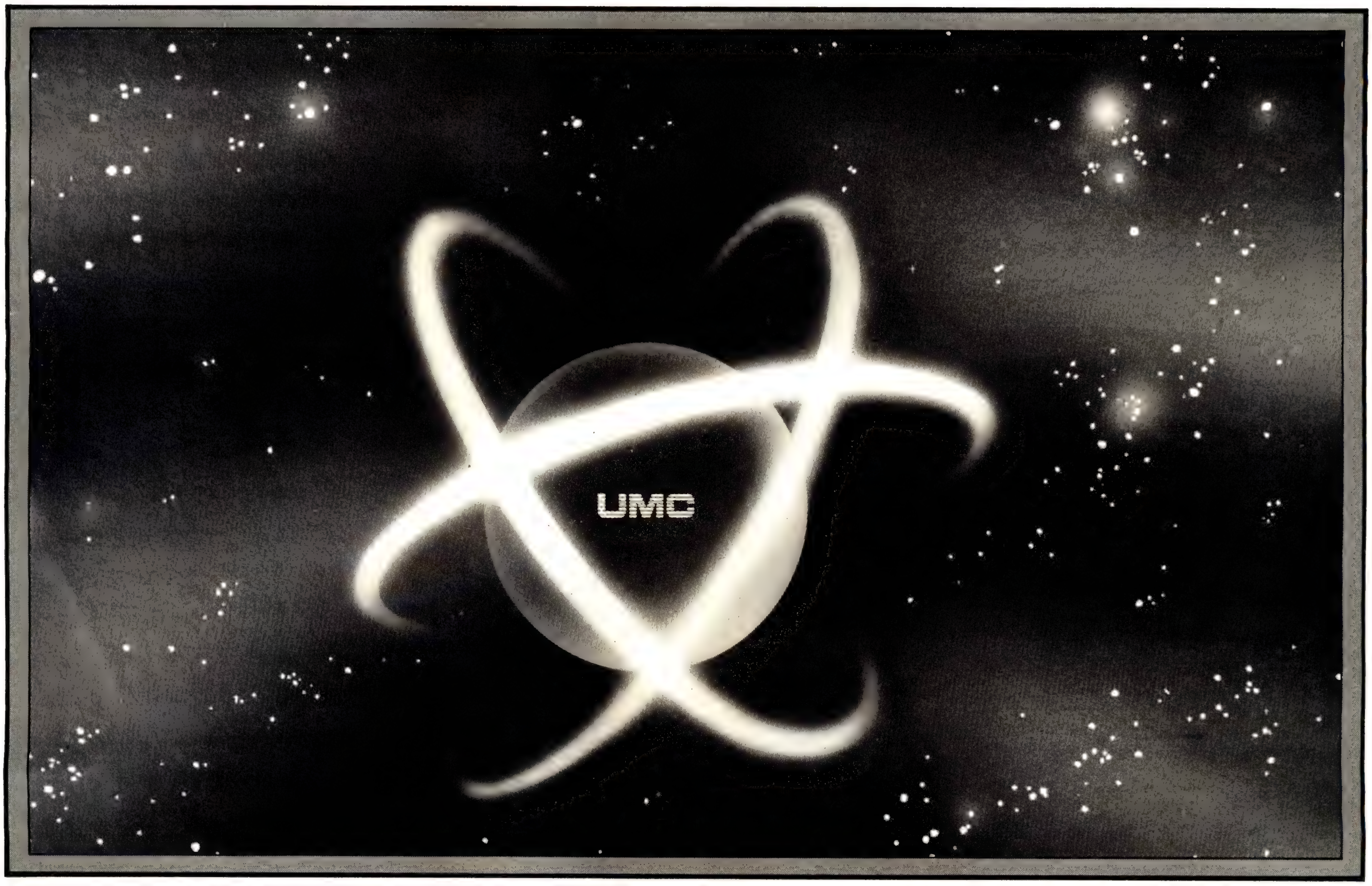
Circle 45 on reader service card

UMC-The nucleus of MOS ICs



UMC, the first IC company in IC industry got break even in the first year of 1982. In 1983, UMC marked a record sales growth rate of 500%.

Among the largest suppliers of MOS ICs, UMC is active in producing computer ICs, communication ICs, consumer ICs and COT (custom owned tooling).

With state of the art equipments, experienced and dedicated IC professionals and sophisticated CAD systems, UMC produces high yields at competitive prices, reliability and on-time delivery.

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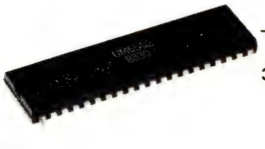

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Circle 46 on reader service card

Confidence growing, U. S. chip makers rush to build capacity

by J. Robert Lineback, Dallas bureau

1984 total expected to rise 30% over the $1.66 billion expended in 1983 as book-bill ratios push to 1.6 to 1.4

With record first-quarter sales casting a strong vote of confidence in continued economic health, U. S. semiconductor makers are embarking on aggressive capital-spending campaigns meant to improve their footing against Japanese-based competitors and to increase market share during the next two years.

Many firms are racing the next downturn—which best estimates place in 1986—to build advanced fabrication lines. But for the time being, chip merchants continue to bank heavily on the notion that business rarely sours in a presidential election year, notes William McClean, research analyst at Integrated Circuit Engineering Corp. (ICE), in Scottsdale, Ariz.

In the first four months of 1984, strong new-order rates—with book-to-bill ratios of 1.6 to 1.4—continue to put tremendous production pressures on chip companies, says McClean, who estimates that Japanese and U. S. firms will spend equal amounts in 1984 to boost capacity. ICE estimates that U. S. firms spent $1.66 billion in 1983, and McClean believes that the total will easily jump by at least 30% in 1984. Many individual firms are reported to be more than tripling their outlays for fabrication lines and assembly plants.

"Even though capital expenditures are being made this year, much of this will not show up in the form of capacity for a couple of years," McClean adds. "But the semiconductor manufacturers don't have much of a choice: they have the money and the demand now."

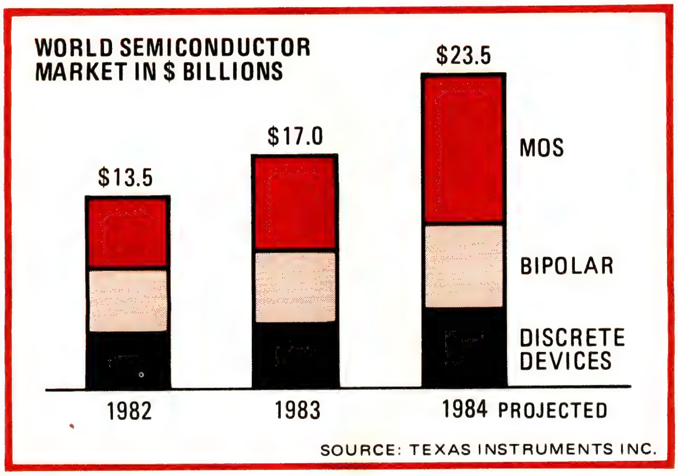
Adding 6-inchers. Texas Instruments Inc., of Dallas, is boosting corporate capital spending to $700 million in 1984, up from $478 million last year. TI declines to say how much is earmarked for semiconductors, but analysts think the firm will spend more than $450 million for new integrated-circuit production facilities capable of using the new 6-inch wafers.

At Motorola Inc., capital outlays for chip plants will also see a big jump, promises James R. Fiebiger, vice president and assistant general manager of the Semiconductor Products Sector, in Phoenix, Ariz. Fiebiger declines to give a 1984 total, but says the increase will "be in the 40%-to-50% range."

"We are still calling 1985 a good year, but probably not [chalking up] the 35% to 40% sales growth the market will see in 1984," Fiebiger says. That estimate takes into account the fact that Motorola and other U. S. firms experienced record sales and orders in the first quarter of 1984. Sales volumes for semiconductor products, paced by 64-K dynamic random-access memories and logic devices, were up 53%, while new orders rose by 80% and backlog advanced by a tremendous 140%, the firm reports.

Hopes for 1985. "In 1985, market growth is shaping up more like 25% to 30%. So our current scenario is for a 1986 recession but a very strong 1985. However, we are still watching the situation very closely because it [a slump] could happen in 1985," Fiebiger quickly adds, voicing the industry's worst fear.

TI president J. Fred Bucy agrees that next year displays all the earmarks of another good cycle but he is not predicting just how good it will be. At TI's annual stockholders' meeting, in April, Bucy placed 1984 world semiconductor sales at $23.5 billion, up 38% from the $17 billion of 1983 (see table). In 64-K dynamic-RAM markets, where Bucy's company



SOURCE: TEXAS INSTRUMENTS INC.

On the move. TI's forecast of world sales shows a 26% increase from 1982 to 1983, but a 38% rise from 1983 to this year. In 64-K RAMs alone, TI sees 1984 totals of 1.2 billion units after 1983's 340 million.

and its major competitors are now promising volume deliveries during the first quarter of next year, demand is expected to grow from 340 million units in 1983 to 1.2 billion units in the peak-volume year, 1986, says Bucy.

In Europe, new-order rates are as high as they have been in the U. S., says Jack Beedle, president of In-Stat Inc., a Scottsdale, Ariz., market-research firm. In a report just released, In-Stat says that during the first quarter of this year, European bookings hit $1.4 billion, up from only $745 million in the same period last year. At the same time, sales rose to $960 million, up from $705 million in 1983. "Europe is becoming a mirror image of where the U. S. was six months ago," Beedle says.

At Mostek Corp., in Carrollton, Texas, officials are more confident of a continued boom market than they were back in December, says Peter Smyth, vice president for North American sales. "We are seeing strength in capital-spending-dependent industries, such as telecommunications, and some of the large computer segments, like minicomputers and mainframes," he says. Last summer, most chip producers credited the personal computer boom with igniting 1983 sales [*Electronics,* Aug. 25, 1983, p. 105], and of them, many remained concerned about the inactivity of large system houses.

At Advanced Micro Devices Inc., in Sunnyvale, Calif., Ben Anixter, vice president for corporate marketing, says, "I think what we now have is a basic fundamental economic boom, which is driven not by the election year but by the desire in industry to have higher productivity." On the strength of that desire, AMD's quarterly earnings from the period ended March 5 were up 360%, to $30.63 million, over last year's period. Sales rose 98%, to $192.2 million.

Solid state

Double-diffusion process for E²PLA could be key to larger alterable memories

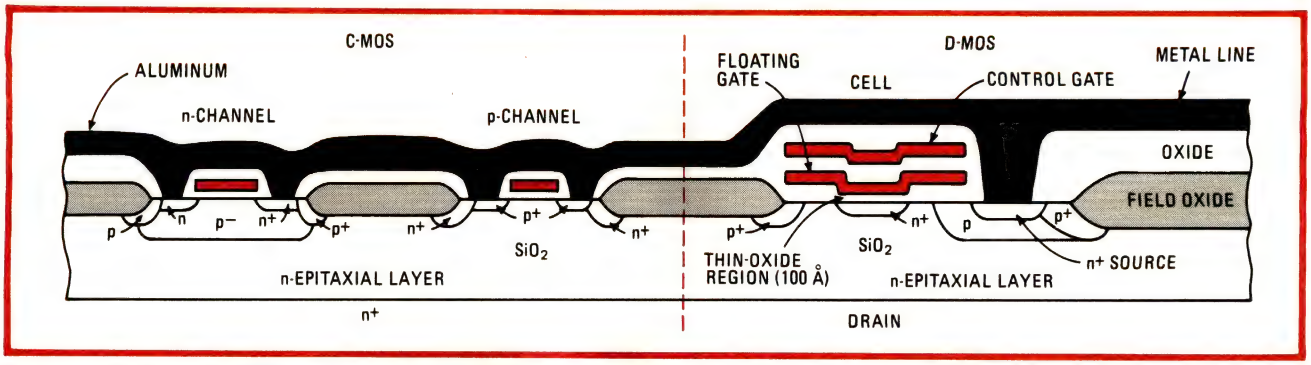
The technology being used by Semi Processes Inc., of San Jose, Calif., to develop an electrically reconfigurable logic array may also open the way to much larger alterable memory chips. The company makes its array with a double-diffusion process that allows the fabrication of very short channels—on the order of a micrometer—and so achieves write times of 50 microseconds or less. Mask-diffused programmable read-only memories are written in milliseconds, and very large PROMs would require very long write times.

Write times matter less for a 2,000-cell logic array than for a 256-K or 1-megabit electrically erasable PROM. Semi Processes was looking for a different kind of performance: fast read times. For some years, the company has used a double-diffused MOS technology to make high-performance field-effect transistors for communications gear, and it paired the fast D-MOS cell with low-power C-MOS to fabricate a test array with a read-erase-write capability [*Electronics,* April 19, p. 41]. The D-MOS transistor takes care of alterations.

"A logic array needs higher performance in the cell than a PROM," says engineering vice president Paul Denham. Semi Processes' array can read logic functions in 70 nanoseconds. "We would have been lucky to get 100 ns with PROM technology."

In place of bipolar. Late this year, the firm will offer commercial versions of its 32-cell test chip as replacements for bipolar arrays. Denham says it is targeted for use "in any system where you want to reconfigure the logic without changing the hardware." He mentions system development, field retrofits, and self-calibrating systems as potential applications. As a bonus, each of the array's cells can be tested nondestructively and then used. Semi Processes speculates that electrically reconfigurable logic could sop up as much as a third of the programmable-bipolar-array market, which it estimates at $500 million.

Other C-MOS firms seem intent on matching Schottky-TTL speeds on the order of 20-ns access times before moving on to the electrically alterable arena. The Cypress Corp., of San Jose, and its nearby Sunnyvale partner, Monolithic Memories Inc., are developing C-MOS arrays with 25-ns access times. Zytrex Corp., also of



Two ways. Cell uses C-MOS for logic and a double-diffused metal oxide structure for read-write-erase. The D-MOS transistor is formed by an n+ source, a floating gate, and an n-epitaxial drain region attached to an n+ substrate, which is attached to a positive supply voltage.

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Circle 18 on reader service card

Sunnyvale, reports that its 1.5-μm process will beat out Schottky at 6 ns. Only start-up Lattice Semiconductor Corp., of Portland, Ore., has plans to introduce an electrically erasable logic chip, but not until next year. "Field-programmable devices will occupy a healthy niche between gate arrays and standard devices," says John G. Posa, Lattice's strategic-marketing director.

Electrical alterability would be far more attractive to ROMs if the write times could be reduced to a practical order of magnitude. Present PROM technology is limited by channel lengths determined by mask size. Semi Processes fabricates its 1-μm channels using 4.5-μm masks.

Lattice will not say how it solved the problem of access and write times for its electrically alterable chips. At least one firm has used diffusion technology to produce fast EE-PROMs. Toshiba's Tokyo Semiconductor Device Engineering Laboratory reports a 256-K EE-PROM, made with a technology much like the one used by Semi Processes, whose cells can be programmed in 3 μs. "We were confident of the technology, but it was reassuring to see that the Japanese tried it too," says one of the firm's designers. **–Clifford Barney**

Research

UCSB courts research partners from industry at a bargain price of $50,000 per year

Say your university is located between two centers of high-tech activity and is working to expand its reputation in science and technology. How do you get the world to notice?

For the University of California at Santa Barbara, 100 miles northwest of Los Angeles and 200-plus miles south of Silicon Valley, the answer has two parts: a $3.1 million award for three years of development work on very fast gallium arsenide integrated circuits [*Electronics,* April 19, p. 42] and a research center that will permit companies to participate for $50,000 a year. (See "Santa Barbara gains in the standings," below)

At the core of the planned center are technologies related to high-speed image processing, a recognized strength of UCSB's department of electrical and computer engineering. "It is the strong common thread tying this research together," says Glen Wade, a professor slated to become the center's director. Even firms that do not actually sell image products use digital-processing techniques, which involve the sensing, capture, storage, and manipulation of data, he says.

Wade calls the $50,000 entry fee "a bargain for research," since it can buy more in a low-overhead university environment, where costs are shared and faculty-graduate student time is relatively cheap. "We're told that university research is from 6 to 10 times more efficient than internal R&D," he says. Other advantages are the real-time examination of research results and ties to faculty and students who will later be prospective consultants and employees.

Industry briefed. The cooperative venture has been put together over a year and a half, spearheaded largely by James L. Merz, associate dean for research development and a professor of electrical engineering. Originally a word-of-mouth promotion, the center was officially unveiled in April for representatives of about 35 companies at a review of the school's research programs. Initial reactions show keen industry interest.

The next step is to seek National Science Foundation seed money for expenses, while UCSB officials hunt recruits for the center. Wade says he expects quick NSF approval, and to launch the center this summer.

Participation is to be interdisciplinary, with some 30 faculty members from six departments expected to take part. Already, 13 specific research programs are listed, with a total of 20 likely to be included in the final proposal to the NSF. Merz says that at least 8 to 10 firms must sign up to get the plan off the ground; the center can hold 50.

Although the center is expected to attract smaller companies, larger ones may deal themselves in, too. "We are as concerned as anyone about getting value for our research dollars," noted a representative of a major aerospace company at the April meeting. **–Larry Waller**

Santa Barbara gains in the standings

Until recently, the department of electrical and computer engineering at the University of California at Santa Barbara has been overshadowed by the two powerhouse departments of the state university system: Berkeley and Los Angeles. Quietly, however, the UCSB department has upgraded itself. The result: its ranking as the most improved program overall among 88 schools studied last year by a committee on the quality of graduate education. The committee, named by the Conference Board of Associated Research Councils, also ranked the department 21st overall for effectiveness. Now the goal is "the top 10 or better," says James L. Merz, associate dean for research development and professor of electrical engineering. The department currently enrolls 600 undergraduates and 240 graduate students. Programs lead to advanced degrees in solid-state electronics, computer engineering, signals and systems, microwaves, optics, and acoustics. **–L. W.**

Communications

Dichroic antenna gets commercial push

Hoping to ride the success of the Landsat-D satellite, which beams data back to earth on two frequen-

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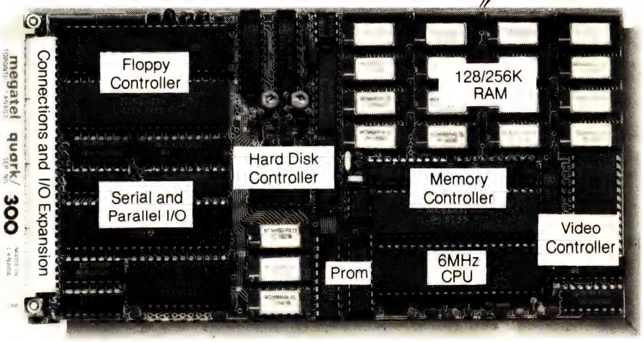

	Quark/100			Quark/150	Quark/200		Quark/300	
MODEL (50 Hz/60 Hz)	021/031	025/035	125/135	025/035	025/035	061/071	025/035	125/135
MEMORY	64K	128K	256K	128K	128K	64K	128K	256K
VIDEO CONTROLLERS ALPHA/GRAPHICS	Monochrome	Monochrome	Mono chrome	Color	Monochrome	Monochrome	Monochrome	Monochrome
LOCAL AREA NETWORK	–	–	–	–	Yes	Yes	–	–
FLOPPY CONTROLLER	5¼ & 8"	5¼ & 8"	5¼ & 8"	5¼ & 8"	5¼ & 8"	–	5¼ & 8"	5¼ & 8"
HARD DISC CONTROLLER	–	–	–	–	–	–	ST506	ST506
SIZE inches millimeters	4x6 100x162	4x6 100x162	4x6 100x162	4x6 100x162	4x9 100x220	4x9 100x220	4x7 100x185	4x7 100x185

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Circle 51 on reader service card

cies, a Southern California firm, Datron Systems Inc., of Chatsworth, has developed a single antenna that can receive both signals. The key to the effort is a dichroic surface for the antenna's reflectors.

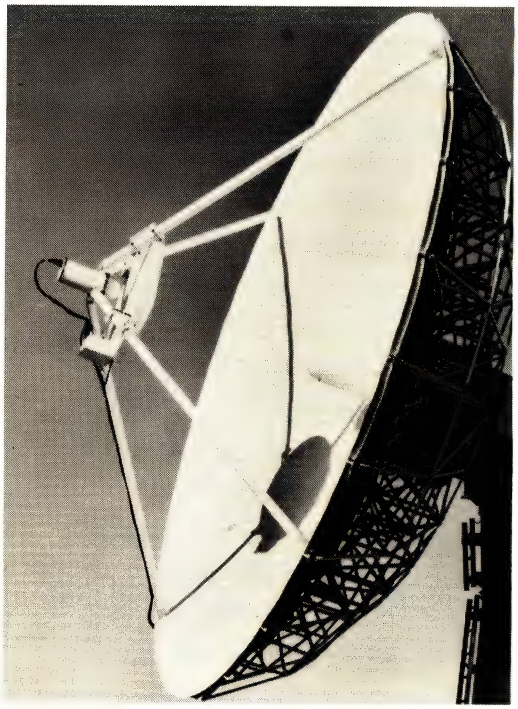
The dichroic material's properties vary so that it is reflective at one frequency and transparent at another, with the frequencies selected according to the size and placement of dipoles in an array on the reflector's surface. Since research on such antennas began in the 1960s, designers have been itching to exploit that two-in-one advantage with the attendant savings in space, power, and money. However, until Landsat took off and started sending its commercially valuable earth-resource data on the X and S bands, applications had principally been limited to airborne military gear and spacecraft.

"Until Landsat, there was no driving program, but we're starting to see a pickup of interest in dichroic equipment," says Herbert Briscoe, Datron's program manager. The economy is clear: one dichroic antenna costs $500,000, or half the million-dollar price tag of two antennas.

So far, limited demand has made the work uneconomical, and coming up with a frequency-selective unit is difficult. What is involved is antenna design by trial and error, followed by painstaking fabrication of materials. The length of hundreds of tiny dipoles that operate on the reflector's surface is crucial, for length determines the exact resonant frequency. Near the resonant frequency, the surface is reflective; at lower frequencies it becomes transparent. No less important is the gap separating the dipoles, called the gap-to-length ratio.

Moment of truth. Computer simulation is fine up to a point, says Briscoe, when a flat surface holding the dipoles must be built and the dipoles' length and gaps tweaked until the best performance is achieved. Another consideration is the maximum incident angle for reflection and transmission, since reflective properties are a function of angle.

Datron found that a gap-to-length ratio of about 1 : 4 worked best; above that, X-band performance tailed off. The final reflector has less than 0.1 decibel loss in the X band (8.025 to 8.4 gigahertz) and less than 0.5 dB in the S band (2.2 to 2.29 GHz).


Dishing it out. Thirty-foot Landsat terminal, operating in X and S bands, has a cassegrain feed with dichroic reflector. It can receive signals at both frequencies.

Says Briscoe: "By far the most expensive and complicated part of development was constructing the entire reflector," which has a 57-inch inside diameter. The process meant stretching a flat copper sheet over fiberglass, bonding it, depositing the dipoles, and then etching the sheet away so that only the dipoles were left. Finally, the assembly had to be pulled into concave shape by a vacuum pump. For anything other than prototype construction, special fabrication equipment would be needed.

One of Datron's 30-foot dishes has been operating since 1982 as a receiver for the Swedish Space Corp. Another is slated to go on the air later this spring in Kenya, where it will transmit in S band for its owner, the University of Rome. The next step for the company is likely to be millimeter-wave equipment and, if demand builds, retrofitting existing antennas. **–Larry Waller**

Computers

CDC shows it means to play in big leagues as it unveils powerful new Cyber 180 family

Signaling its intent to stay in the major leagues of general-purpose computing, Control Data Corp. late last month replaced its Cyber 170 series mainframes with a new family. The Cyber 180 includes a top-end machine—the Cyber 180 Model 990—that in a dual-processor configuration is rated at more than twice the performance levels of International Business Machines Corp.'s biggest computer.

CDC does not in fact rate its machines in terms of millions of instructions per second (MIPS). Other performance figures supplied by the Minneapolis firm do, however, indicate that the two-processor Model 990 rates at 58 MIPS. That figure can be compared with the 29-MIPS range of IBM's largest 3080-family system and also puts Control Data's machine some 29% ahead of the previous general-purpose performance champion, the 45-MIPS M382, from Japan's Fujitsu Ltd.

As an added feature, the 990 incorporates vector as well as scalar processing capabilities, a first for a general-purpose mainframe. With a capability of about 120 million floating-point operations per second, the 990 cannot match the 800 million floating-point operations per second claimed for CDC's Cyber 205 supercomputer but does nonetheless re-

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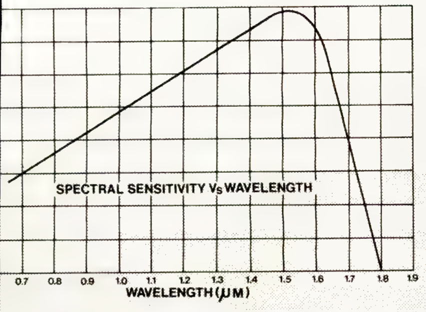

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Circle 53 on reader service card

News briefs

RCA disk-storage technique uses three lasers on a chip

By using three semiconductor lasers on a single chip, RCA Laboratories, in Princeton, N. J., has developed a technique to record information on an optical disk. RCA says that the method, called multichannel recording, is "considered a major step in the development of a compact system that can restore vast amounts of information at extremely high speeds." The disk, with a 14-in. diameter, can store as many as 100 billion bits of data. The system's diode lasers, fabricated with aluminum gallium arsenide, are constricted double-heterojunction models with large optical cavities.

TI reports big profits on sales of home computers—finally

What a difference just one year makes. Last May, Texas Instruments Inc. was still actively marketing its ill-fated 99/4A home computer. Sales took a nose dive that month, eventually pulling the entire Dallas corporation into the red. But after officially withdrawing from the home-computer business last fall [*Electronics,* Nov. 17, 1983, p. 104], TI is at last making profits in the consumer market—although not intentionally, according to its officials. At April's annual stockholders meeting, TI reported that its clearance sale of discontinued 99/4A products contributed a net income of 41¢ a share during the first quarter of 1984. Companywide, total profits were $79.8 million, or $3.32 a share, on sales of $1.34 billion. Last year, corporate revenues of $1.17 billion brought in profits of $7.1 million.

Ford Aerospace adds a Space Information Systems division

Believing that U. S. space activities are taking off once again, Ford Motor Co.'s aerospace subsidiary is increasing its presence in the Houston area by creating a Space Information Systems division to service the growing business at the Johnson Space Center. Ford Aerospace & Communications Corp. now has some 1,400 employees in Houston, where it has operated and supported mission-command-and-control systems at Johnson since 1962. Ford cites the successful operation of the space shuttles and the planned development of an $8 billion space station as the key factors in its decision.

Wang's FastLAN eases the link to a broadband local net

Citing the need to ease the interconnection problem in broadband local networks, Wang Labratories Inc., of Lowell, Mass., last month introduced FastLAN at the Second Annual Broadband Local Networks Forum, in Washington, D. C. FastLAN—a set of three modules that will help small-to-medium-sized users hook up to broadband local nets without custom cable installations—opens the technology "to the low- and middle-end user," the manufacturer claims. By applying the correct mix of amplifier modules, network branch modules, and multiuser outlet modules, 4 to 640 transmit/receive ports can be tied together in a stand-alone local net or linked to a larger backbone network. A Wang spokesman says that the cabling scheme is particularly appropriate for renters, since its modular design makes it easy to move.

California leads in electronics firms—N. Y. is second, Mass. third

California, the home of more electronics companies than any other state, has more than four times as many as second-ranked New York, according to a recent survey by the American Electronics Association. The AEA's first such breakdown shows California with 4,054 firms, followed by New York with 948 and Massachusetts with 937. Rounding out the top 10 are New Jersey (555), Illinois (458), Texas (445), Minnesota (369), Pennsylvania (351), Oregon (338), and Florida (334). At the bottom are West Virginia, North Dakota, Wyoming, and Hawaii, with three each, and Alaska and Puerto Rico, each with one.

flect CDC's commitment to providing more scientific-computing capabilities in its general-purpose line.

Calling the announcement "the biggest deal for Control Data Computer Systems since we announced our first product, in 1957," the division's vice president, Larry E. Jodsaas, notes that the Cyber 180 is "the beginning of a brand-new system and architecture that will last easily through this century."

Six in brood. In all, the family includes six models—three also offered with dual processors—beginning with the model 810 superminicomputer. As a replacement for the current $400,000 Cyber 170 model 815, the 810 will offer performance in the 1-MIPS range and is positioned to compete against the VAX 780 family, from Digital Equipment Corp., Maynard, Mass.

Unlike the 815, which requires 400-cycle power for operation, the air-cooled 810 operates on 50-to-60-hertz power and costs about $250,000 for a typically configured system with 2 megabytes of main memory. (Up to 16 megabytes, at a cost of $7,500 a megabyte, are available.) This model is aimed at distributed office environments "where the VAX has come in and grabbed a lot of the business out of CDC Cyber accounts," as Jodsaas puts it. The 810 will compete against VAX models that cost from $195,000 to $400,000, Control Data sources say.

A key feature of the Cyber 180 line is its multistate architecture, which allows all the members of the family to run CDC's 20-year-old Network Operating System (NOS) simultaneously, as well as a new one, NOS/VE (for virtual environment). This maintains a migration path for existing CDC customers, while for the first time providing the company's mainstream products with virtual memory.

With a virtual-addressing space of as many as 8,800 gigabytes, NOS/VE will answer customer complaints about NOS, which has an upper-limit addressing range of 15 megabytes. Unlike the 60-bit word format used with NOS, the new virtual operating system is based on indus-

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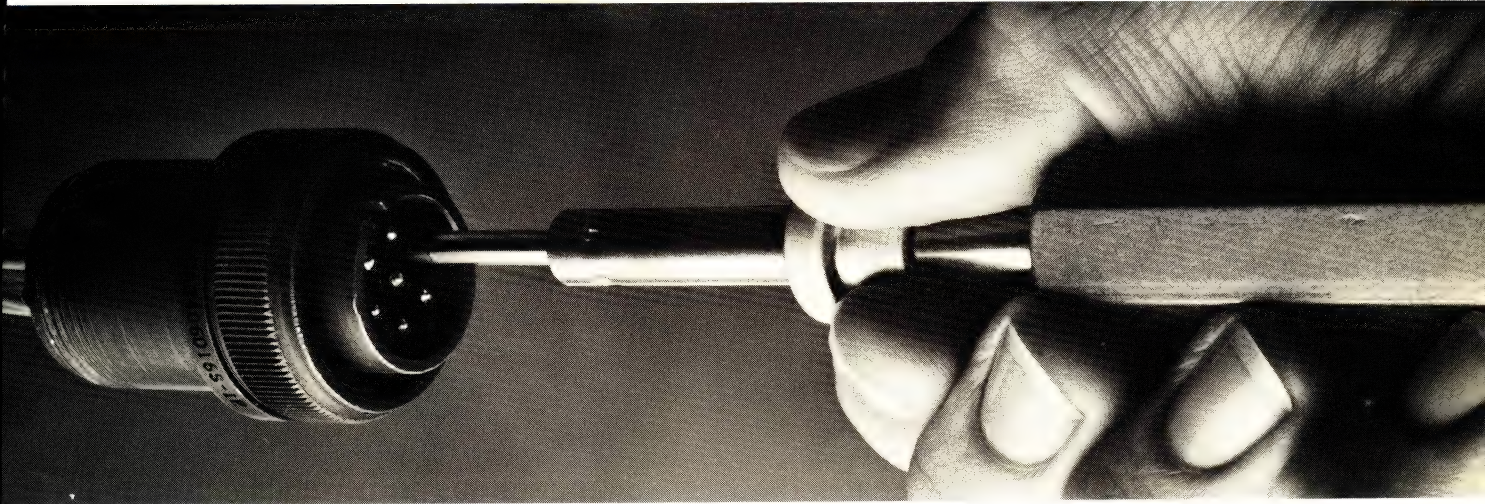

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try-standard 8-bit bytes and 64-bit words, so application programs from other vendors can easily be adapted for use on the Cyber 180, Jodsaas points out. Additional versatility is provided through support from AT&T Bell Laboratories' Unix operating system Version V, which will be offered as a subsystem under NOS/VE.

Other Cyber 180 features include a data-base management system called IM/VE (information management/virtual environment), which features a three-schema, fully relational data structure; a baseband networking system known as CDCNET, for local and geographically dispersed resource sharing; and NOS/VE support for a broad range of high-level languages, including Cobol, Fortran, APL, Sort/Merge, Pascal, Lisp, C, and Cybil (a Pascal-based CDC language). The Cyber 180 architecture also includes a number of hardware-based security features previously implemented in software. Jodsaas claims that they will make NOS/VE the most secure operating system on the market.

Three models in the Cyber 180 family—the 835, 845, and 855—have been sold previously in the 170 series and are still available. Two new models, the 810 and 830, are to be shipped in July. The top-end 990 will be available in mid-1985 at a cost of about $6 million for a fully configured single-processor system with 16 megabytes of main memory.

With the maximum 32 megabytes, a single-processor 990 will cost $7 million to $8 million. Prices for the dual-processor version have not been set. All models in the family rely on a microcoded central processor. Models 835 and up are liquid-cooled.

–Wesley R. Iversen

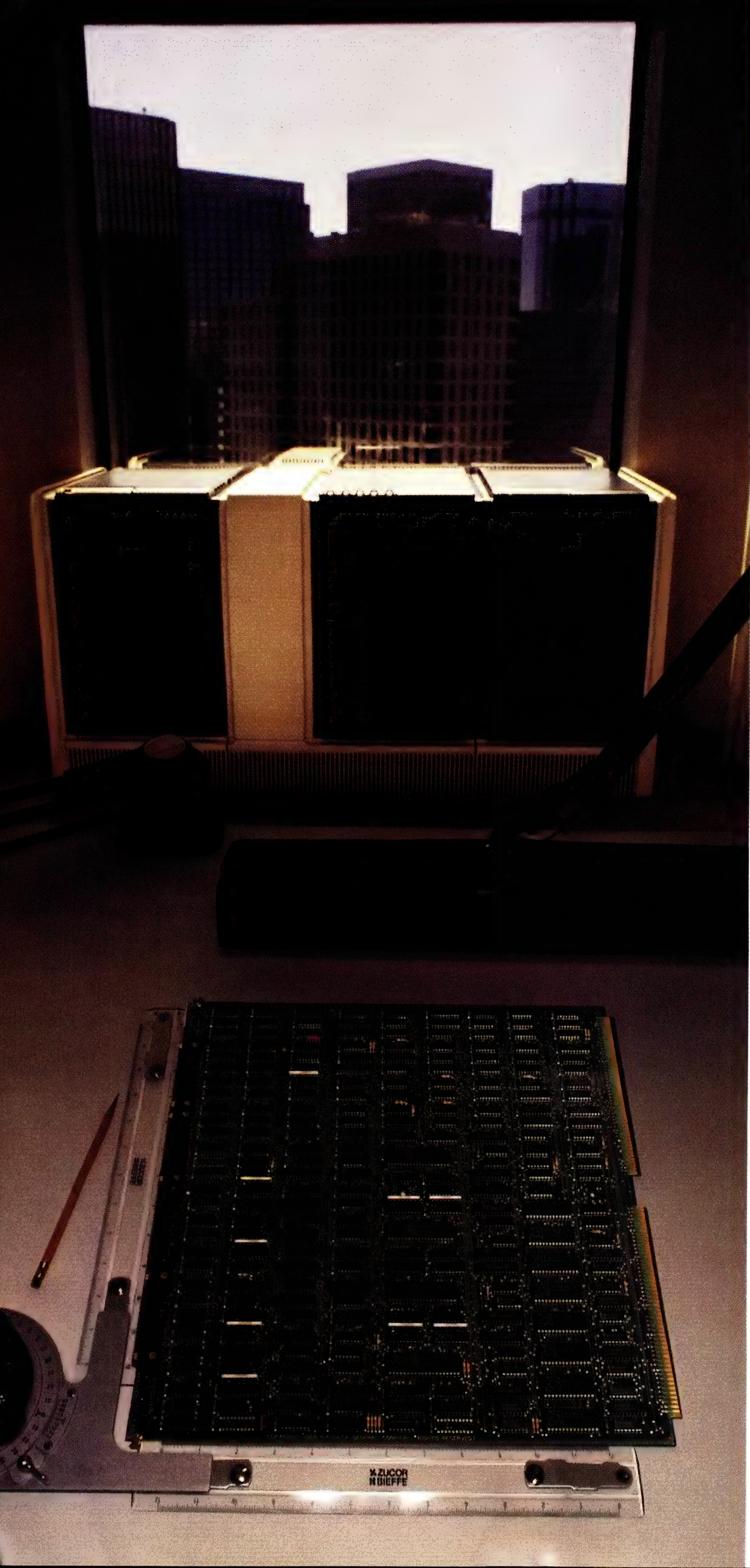
Memories

Dynamic RAM helps design for speed

A couple of nanoseconds' head start when setting up row addresses in dynamic random-access memories can

Texas Instruments and Data General push supermini performance to new heights.

- **TI's Advanced Schottky Family** includes the industry's highest speed TTL logic, which helps double throughput of new DG state-of-the-art-designed superminicomputer (*Page 2*).
- **Performance Budgeting** options—available only with TI's Advanced Schottky Family of ALS/AS devices—optimize your system speed/power product (*Page 3*).
- **Having over 240 functions today with more to come,** TI's rapidly growing ALS/AS Family maximizes your design options in high-performance TTL logic (*Page 4*).▶



TI's high-
supermini

When it came time to design a virtual-memory 32-bit superminicomputer unmatched for performance, Data General logically turned to Texas Instruments for semiconductor logic. And TI came through.

By designing-in high-speed AS logic functions from TI's Advanced Schottky Family, Data General was able to introduce its new ECLIPSE MV/10000™ superminicomputer a year ahead of the industry. And achieve a blazing machine cycle time of 140 ns.

Speed increases from 45 ns to 32 ns

The TI 'AS881, a 4-bit arithmetic logic unit/function generator, got the MV/10000 off to a flying start. Far faster than standard Schottky, it reduced the delay time of a 32-bit ADD operation from 45 ns to 32 ns. Plus, its 24-pin, 300-mil-wide package required 50% less board space.

TI's high-speed 'AS882, a 32-bit look-ahead carry generator, also proved crucial to the supermini's state-of-the-art design. It integrates a 32-bit look ahead on a single chip.

Strong support speeds supermini to market

From an initial presentation . . . to meeting specs . . . to producing devices . . . to testing . . . to on-time delivery, TI gave Data General its full support and cooperation.

All of which helped Data General get its new supermini to market a year early.

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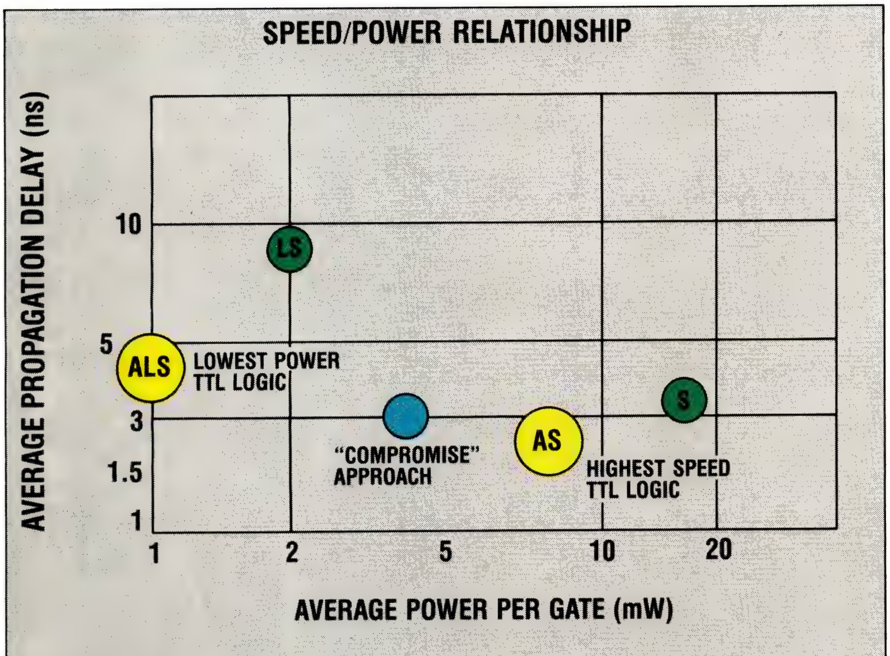
◀ **For maximum speed,** DG's new ECLIPSE MV/10000 32-bit superminicomputer incorporates 51 TI high-speed AS logic devices—46 'AS881s and five 'AS882s. A versatile, high-performance computer system, the MV/10000 can be used on a wide variety of design projects. Cover example: Development of plans for a skyscraper involving simulation of various physical forces on the structure.

speed AS logic speeds DG's off the drawing board...at 140 ns!



Performance Budgeting—specifying Advanced Schottky Family ALS and AS devices on a socket-by-socket basis for optimum combination of speed and power—allows designers to achieve outstanding performance levels in a wide range of state-of-the-art system designs.

Performance Budgeting: The key to optimizing system speed/power product.

Why compromise your design with too little TTL speed? Or too much power? Instead, get the highest speed and lowest power with TI's Advanced Schottky Family of ALS/AS devices. Put TI's Performance Budgeting to work for you.

Performance Budgeting means you can place AS devices in the critical speed paths to take advantage of their fastest speeds, while spotting ALS devices where you can make the most of their lowest power.

By specifying socket by socket, you can achieve the optimum combination of system speed, power, and economy.

AS functions: World's highest speed TTL

When speed is your top TTL priority, TI's AS logic is your best choice. With a typical 1.7-ns gate delay and only 8-mW power dissipation per gate, AS logic is faster than a compromise approach to TTL (see above and at right). And TI offers you a wide choice of AS logic devices.

In addition to the high-speed 'AS881 and 'AS882 devices used by Data General, there are also the following new, very fast, 8-bit, byte-oriented ICs:

'AS870/'AS871 register files contain internally multiplexed, dual, 16-word by 4-bit data sources for direct ALU input. Plus, multiplexed I/O ports minimize processor data-path access times to memory and system bus structures.

The 'AS877 octal transceiver provides both parallel and serial ports for system interconnection. Its integral serial data port simplifies fault detection and reduces system debugging.

'AS867/'AS869 octal bidirectional counters are fully paralleled, high-performance, presettable 8-bit counters that minimize next-address generation compromises. Both asynchronous and synchronous clear versions are offered.

Many more AS logic devices available from your TI distributor are listed on the next page.

ALS functions: Lowest power TTL

Is low power your key TTL requirement? Then TI's ALS devices are your best solution. They give you absolutely the lowest power—1.2-mW gate power dissipation—plus very respectable speed at 4-ns gate delay, typically. ALS logic typically requires 68% less power than a compromise-logic approach, with only 25% less speed.

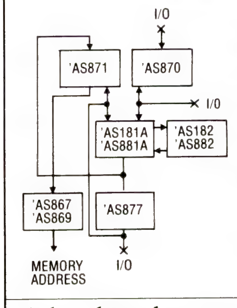
TI packaging options include unique 68-pin plastic chip carrier

Need higher complexity functions for your new designs? Or pin-for-pin equivalent functions for easy system upgrades? TI's broad Advanced Schottky Family of ALS/AS devices gives you both.

Most members of the Advanced Schottky Family are available in 14-pin, 16-pin, 20-pin, and the new 300-mil-wide, 24-pin DIPs. Also, the family now comes in surface-mount 20-pin, 28-pin, 44-pin, and TI's unique 68-pin plastic-leaded chip carriers.

Arithmetic Processor

TYPICAL DATA PATH
Throughput Time (ns)



Word Length	8 bit	16 bit	32 bit
Register File	12	12	12
ALU	10	14	19
Accumulator/ Address Generator	10	10	10
Total Throughput Time	32	36	41

Higher throughput at the component level and more architectural features enable you to increase overall system performance with TI's high-speed AS logic.

Use of the new surface-mount chip-carrier packages can almost double functional densities. Board space can also be reduced by using the new 300-mil-wide, 24-pin DIP versus the industry-standard 600-mil-wide package.

For more information on TI's Advanced Schottky Family of ALS/AS logic, return the coupon on the next page.

See back page for more information.

Texas Instruments Advanced Schottky Logic Family Today

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37401BCB	54ALS08
37402BCB	54ALS11
37501BCB	54ALS32
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go a long way toward breaking the 100-ns access barrier for faster storage in systems using these parts. That is the reasoning behind a recently modified static-column-decoding scheme from Inmos Corp., slated to debut later this year on complementary-MOS dynamic RAMs.

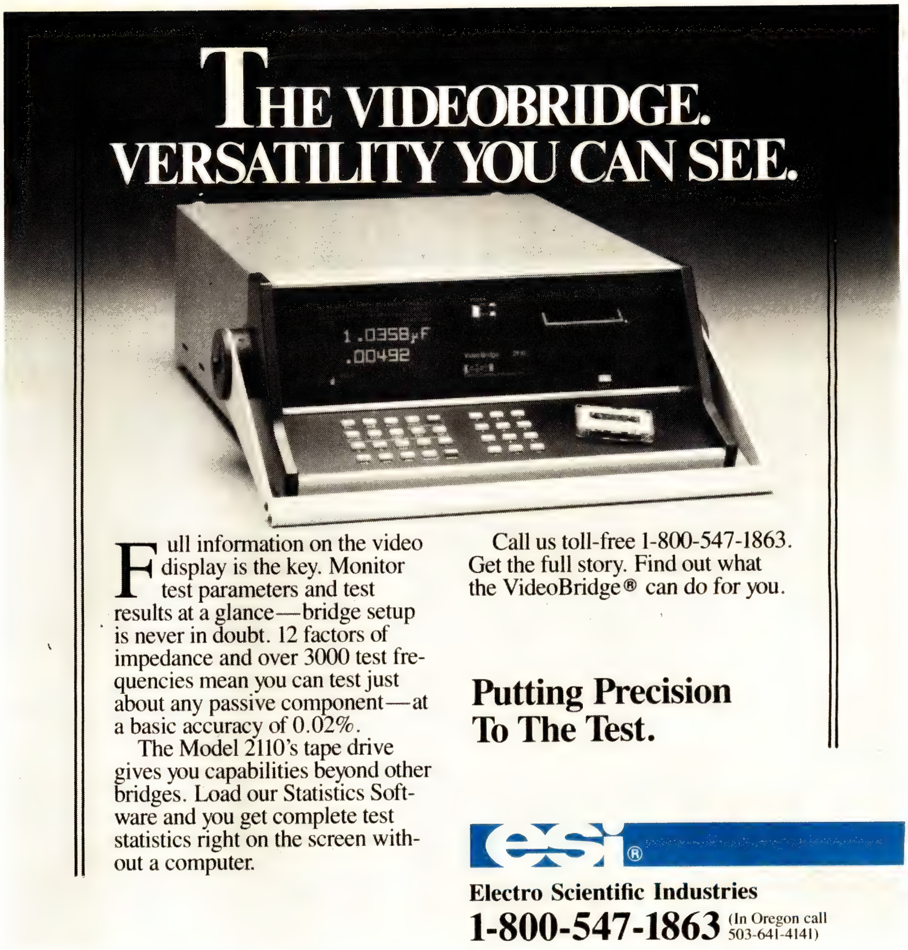
Using a fuse-programming technique to set the new option, Inmos plans to offer the scheme on high-speed 256-K RAMs as well as its next-generation 64-K C-MOS chips. The Colorado Springs, Colo., company says the new addressing plan will help systems designers get maximum speed out of dynamic RAMs by eliminating the series of critical timing windows usually associated with calling data from memory arrays.

This is done by adding a 2-ns set-up time at the start of a row-address capture period. The result is a greatly reduced hold time, allowing the chip to complete row-address capture in about 4 ns, compared with 15 ns in some existing chips.

Moving in. With many dynamic-memory makers striving for ever-increasing access speeds, static column-addressing techniques have already found their way into a number of high-density C-MOS designs. Most recently, Intel Corp. introduced such a feature on its 100-ns 51C65. In Japan, Fujitsu Ltd. is also producing 100-ns 64-K dynamic RAMs featuring static column addressing.

Compared with more conventional approaches, static column decoding actually begins accessing the column address prior to the clocking of the column-address strobe. This allows the chip to ripple quickly through the sequence of addressing events without waiting for the column-address strobe to latch the column-access signal. The addressing scheme—easier to implement in low-power C-MOS than in n-channel technology—makes low-cost dynamic chips appear more like their faster static-RAM cousins.

But as dynamic memories get faster, computer designers are finding it more difficult to actually achieve minimum access speeds in their systems, says Fred Jones, strategic memory marketing and applications



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manager at Inmos. A 100-ns access barrier now exists for most systems, he adds.

A key hurdle is inherent propagation delays associated with multiplexed row- and column-addressing signals—traditionally in dynamic RAMs to reduce pin counts and keep packages as small as possible. As the multiplexed series of critical timing edges is compressed, some parts of the addressing sequence can be skewed, preventing systems designers from pushing their designs to the upper speed limits of the high-performance parts, says Jones.

"As dynamic RAMs get faster, we are finding that we are starting to bump into the boundaries of how fast signals can be multiplexed," Jones notes. "So just making a part significantly faster provides very little, if any, system advantage."

At the start. One solution, Inmos believes, is changing the row-address setup period at the start of a static column-decoding cycle to a slightly positive value. Traditionally, addressing cycles have guaranteed 0-ns row-address setup times, meaning signals can be valid just at the time when the latch is set by the row-address strobe. To do that, however, means a row-address hold period of 8 to 15 ns before the RAM can switch to column addressing.

The problem is coordinating the series of address-timing edges when propagation delays off-chip drive logic. "You cannot change the output logic level of a device in 0 ns," Jones explains. "It takes some finite length of time for electricity to propagate. Typically, the minimum delay in TTL devices is 2 ns.

By using a slight-positive setup period, Inmos believes it has replaced the series of critical edges with a single 2-ns setup period at the start of a cycle. "This will allow systems designers to achieve very high performance without being forced to violate certain parameters and hoping it will all work out," Jones states.

In addition to the modified static column-decoding option, Inmos will utilize some of the same addressing principles in an extended-page mode on its 256-K-by-1-bit dynamic RAM,

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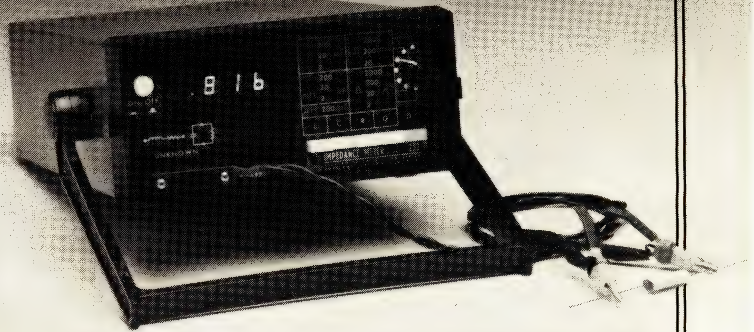

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Electronics report

now slated for samples in the second half of 1984. It will set either option for customers by blowing on-die fuses after the chips are assembled. –J. Robert Lineback

Personal computers

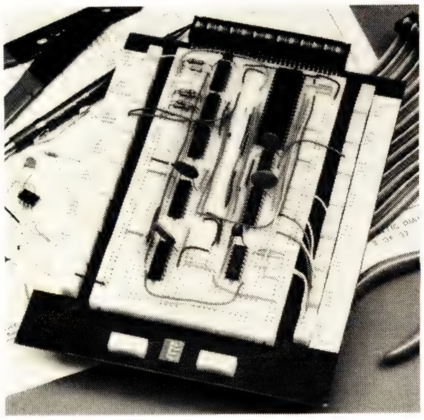
Board speeds prototyping job

The burgeoning field of new applications for personal computers could expand even more if a faster and cheaper way of doing a laborious development job takes hold. In this instance, it is a simpler method of building prototype interface boards with which personal computers can perform robotics tasks, process control, and similar jobs.

The eZ Board, invented by a tiny firm in Anaheim, Calif., connects directly into the computer's bus-expansion slot and offers a breadboarding area with block-array sockets where 16 components can be plugged in, sans solder or Wire-Wrap. An engineer can easily change the configuration and test each version in real time through the computer.

The current method of breadboarding involves trial and error: fastening and removing components on a bare board, attached either by soldering or Wire-Wrap, and then following through with repeated testing.

"We call it a solderless experimen-



Easing the way. EZ Board plugs into a personal computer's bus expansion slot to help engineers build prototype interfaces for such jobs as robotics and process control.

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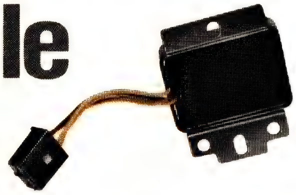

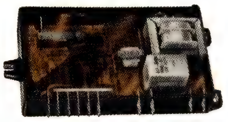

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tal tool, which is really a form of revisable hardware," says Rahim Sabadia, president of the Sabadia Export Corp., who devised the eZ Board with an associate. He estimates it cuts the time and expense of breadboarding to perhaps a tenth.

A manager of industrial engineering at neighboring California Computer Products agrees that the board offers important savings. "It could be the shortest distance between a piece of paper with a circuit design and a working interface," says Marcus M. Porter. "It looks to be a really useful development tool, especially in pulling signals out of a bus." He expects to put the board through its paces in his laboratory when it becomes more readily available in quantity.

Four areas. EZ Board routes functions from each of the computer bus's output terminals into the breadboard area, where each is clearly identified and accessible. The board has four distribution areas, each with 50 tie points for power, ground, clock lines, and reset commands, among others. A four-position switch in a dual in-line package has each position connected to each distribution area. Sabadia's board works with computers from IBM, Apple, and Commodore—about 80% of the personal-computer population.

Like many ideas that lead to products filling a need, the eZ Board was an invention of necessity. Sabadia and Rafe Hosain, an electrical engineer moonlighting from a nearby military electronics firm, needed an interface board for a robotics project they were pursuing and found none existed. After devising and demonstrating their board late last year, they decided to offer it as a product and have applied for a patent.

At $175, including an 18-inch flat-ribbon cable and connector, the board is not much more expensive than the conventional materials required in breadboarding, says Sabadia. His firm is selling the board directly and plans a larger one that holds more components, along with buffers and decoders as options. There also will be a line of add-on interface boards to be offered in 1984. **–Larry Waller**

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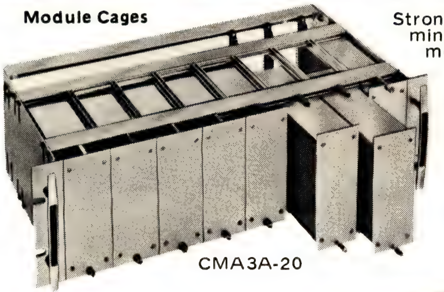
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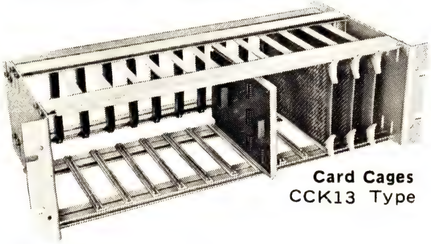
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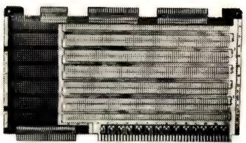
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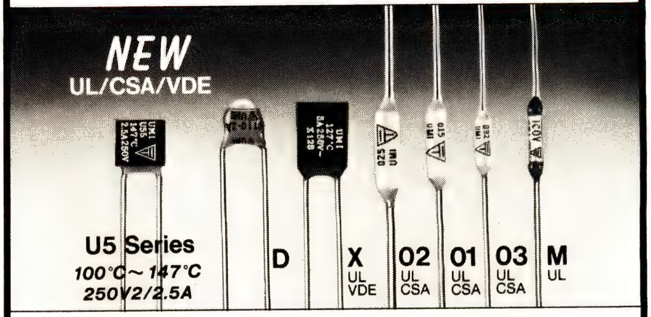

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SDM 5013 1)	160	1000 Min	4.0	100	1.5	1.0	150	T0-3
2N 3773	140	15/16	8.0	100	1.5	1.0	150	T0-3
2N 3772 2)	60	15/60	10.0	60	2.5	1.0	150	T0-3
2N 3771 2)	40	15/60	15.0	40	3.75	1.0	150	T0-3
2N 6254	80	20/70	5.0	80	1.87	1.0	150	T0-3
2N 3055H 2) 3)	60	20/70	4.0	60	1.95	1.0	117	T0-3
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Washington newsletter

Telecom imports soar as result of AT&T breakup

The breakup of American Telephone & Telegraph Co. is having "enormous and unanticipated effects on increasing imports" of telecommunications equipment, the International Trade Commission has been told. Rolm Corp., the Santa Clara, Calif., equipment maker, warned that the seven new regional telecommunications companies represent powerful markets that should not provide "unfair advantage to offshore manufacturers." The Electronic Industries Association was more direct, claiming that **the U. S. telecommunications-equipment trade balance remained positive and growing from 1977 to 1982, turning to a deficit only in 1983 as a result of imports from Japan.** Last year's $240 million deficit in telecommunications equipment—imports rose to $1.075 billion, compared with exports of $835 million—resulted from Japanese imports, which account for 45% of all imports to the U. S., says the EIA. That is "more than twice the share of any other country."

NBS to press compatibility among computers

Striving to hasten the coming of computer compatibility, the National Bureau of Standards says that by year end it will start enforcing Federal Information Processing Standards for Government computers. The aim is to encourage voluntary adoption of the standards for commercial markets. At the July 9–12 National Computer Conference, **the bureau will join 16 computer makers, chip designers, and users in a demonstration of the Class IV transport protocol** of the International Standards Organization's Open System Interconnection model. There will be two local-network technologies: carrier-sense multiple access with collision-detection, for business, and a token-bus protocol, for process control.

Comsat to push product sales

Communications Satellite Corp., planning to leverage the technological prowess of its three product divisions, is going to raise its manufacturing profile and could make low-cost Ku-band transmit-and-receive terminals one of its first products. **The three Comsat subsidiaries—Telesystems, Amplica, and Compact Software—"have never made money for us to date,"** says A. William Perigard, president of Comsat Technology Products. "My goal is to drive them into profitability," he says. An Advanced Technology section reporting to Perigard has been set up to identify and market the new integrated products, which will be designed by Comsat Labs and manufactured by the three companies.

Patent Office to spend $300 million to automate

Planning Research Corp. will handle the design, implementation, and maintenance of the Government's largest document-storage and retrieval system to date under terms of a $300 million contract from the U. S. Patent and Trademark Office. The McLean, Va., computer-services firm says it plans to buy some $130 million worth of computer hardware—including 2,000 work stations and optical disk-storage devices—and to subcontract software development to Chemical Abstracts Service, of Columbus, Ohio. **Automating the office's 25 million documents will require memory capacity in excess of 12,000 gigabytes,** notes a Planning Research spokesman. The goal is to have a paperless system on line by 1990, so that examiners will be able to process and issue patents and trademarks within 18 months—as opposed to the current 27 months.

Washington commentary

Trade strategies for the future

What began during the trough of the recession as a call by Democrats to protect U. S. markets and jobs by developing a "national industrial policy" was laughed at by most Republicans as just so much liberal rhetoric. But that was before a presidential election became an immediate concern. When Republicans began electioneering in earnest, they, too, seized on the issue, giving it a new name. And that is how President Reagan came to appoint a Commission on Industrial Competitiveness.

The commission's report is not yet in, nor are its recommendations likely to influence the outcome of November's election. However, within the upper echelons of business and labor, America's ability to compete in global markets seems certain to remain a hot issue for the foreseeable future. Hardball is the name of the game in world markets that are becoming increasingly sophisticated; as the Committee for Economic Development (CED) points out, "the era of unquestioned U. S. dominance in the world economy is clearly over, and has been for some time." CED, a blue-ribbon collection of U. S. industrial leaders, is now making known its views on U. S. industrial competitiveness as it puts forth its strategy in a new statement.

Freedom to compete

Not surprisingly, CED's "Strategy for U. S. Industrial Competitiveness" is to let the private sector fight it out in world markets, while letting America's world competitors know that U. S. industry has the strong support of its government. One example of that support would be tougher and faster enforcement of U. S. trade laws—including countervailing tariffs—against foreign companies that unfairly target U. S. markets. More important, CED wants the U. S. to push harder for more flexible export guidelines on high technology, so that new and developing markets will not be sacrificed in the name of national security [*Electronics,* April 5, p. 58].

Competing countries have "very skillfully used" perceptions of American inconsistency on high-tech export policy to discourage potential foreign customers from buying U. S. products, argues Edmund B. Fitzgerald, vice chairman of CED's trade subcommittee, "because of our alleged inability to guarantee long-term product support." (Fitzgerald is president of Northern Telecom Ltd.)

To eliminate from export-control lists many of the estimated 1,200-plus products whose sale abroad can be challenged on national-security grounds, Franklin Lindsay, of Engenics Inc., a genetic-engineering firm, has come forth with a novel "sunset law." Lindsay, long familiar with Defense Department contracting rules, would "automatically remove each technology or product from the export-control list after four years unless the Government presents evidence that the specific control is still essential to national security." Despite the probable effectiveness of Lindsay's proposal in such areas as electronics, the military is not likely to give it consideration.

Monitoring competitors

However, another CED recommendation seems better attuned to the politics of an election year and supportable by all parties. That is the call for the creation of a new Government office to "monitor innovation and competition policies in each major country," including government-subsidy practices. While the Commerce Department contends that it is already doing this, Government and industry officials agree that the job could be done much better with far less fragmentation of effort. Japan and the UK already have such offices—neutral and central sources of information and analysis. CED believes that such an office could put international competitors on notice that the U. S. Government "is seriously concerned about foreign subsidies and will consider [remedies for] unfair trade."

Unfortunately, little has been said and less written about trade as an election-year issue. Although the subject ranks near the top of most savvy politicians' list of important problems facing the nation's economy and the continuing recovery, candidates find talking about trade dull and are convinced that most voters couldn't care less about the whole thing.

Certainly, CED's proposals for industrial competitiveness provide little grist for television's news mill. But that is not to say that electronics managers or engineers wouldn't find a good deal of information and food for thought—and perhaps encouragement to look at their jobs and products in a different light. How the U. S. responds during the next few years to the trade challenge will have far greater impact on the structure of its domestic society than virtually any other issue.

–Ray Connolly

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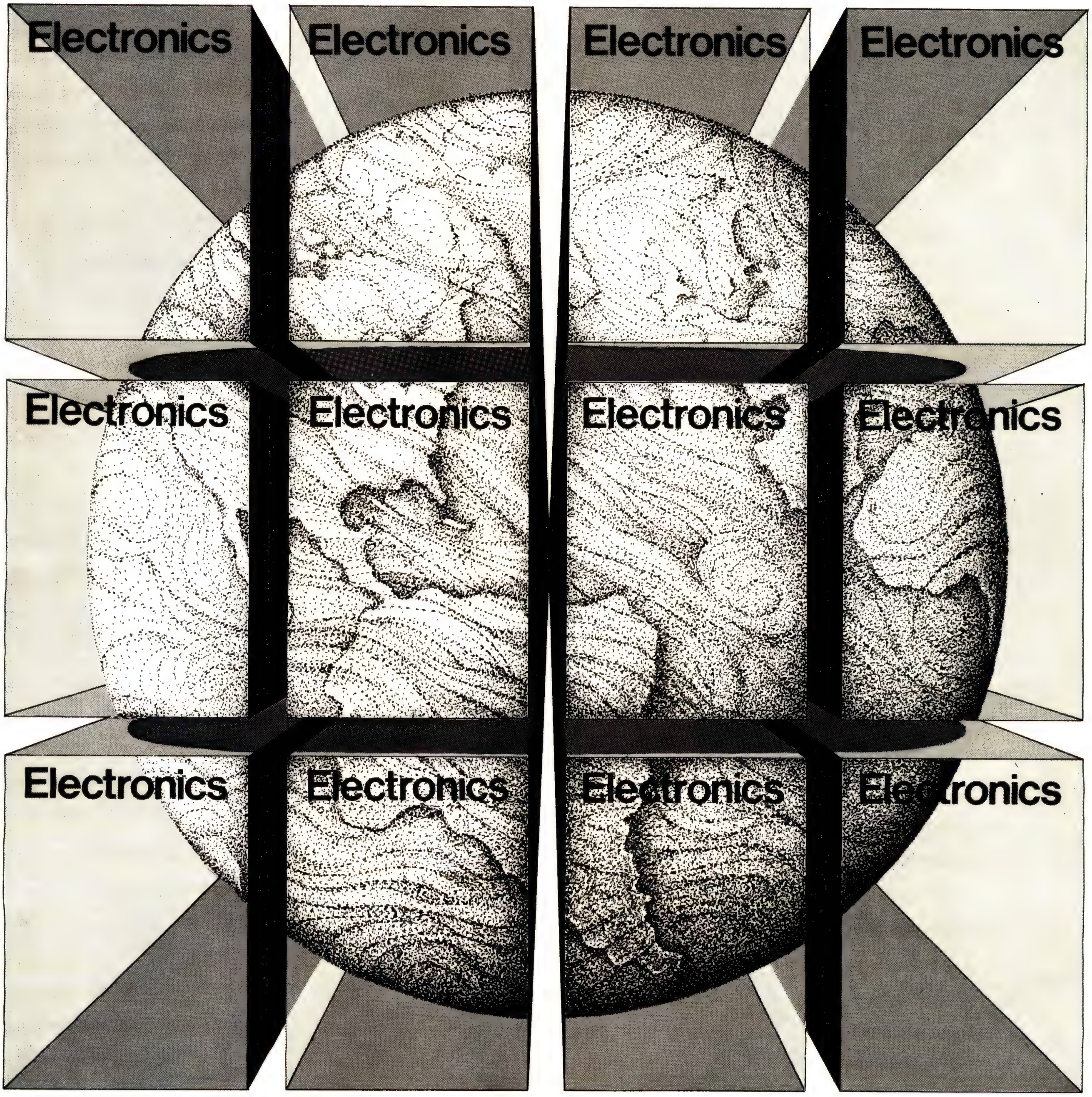

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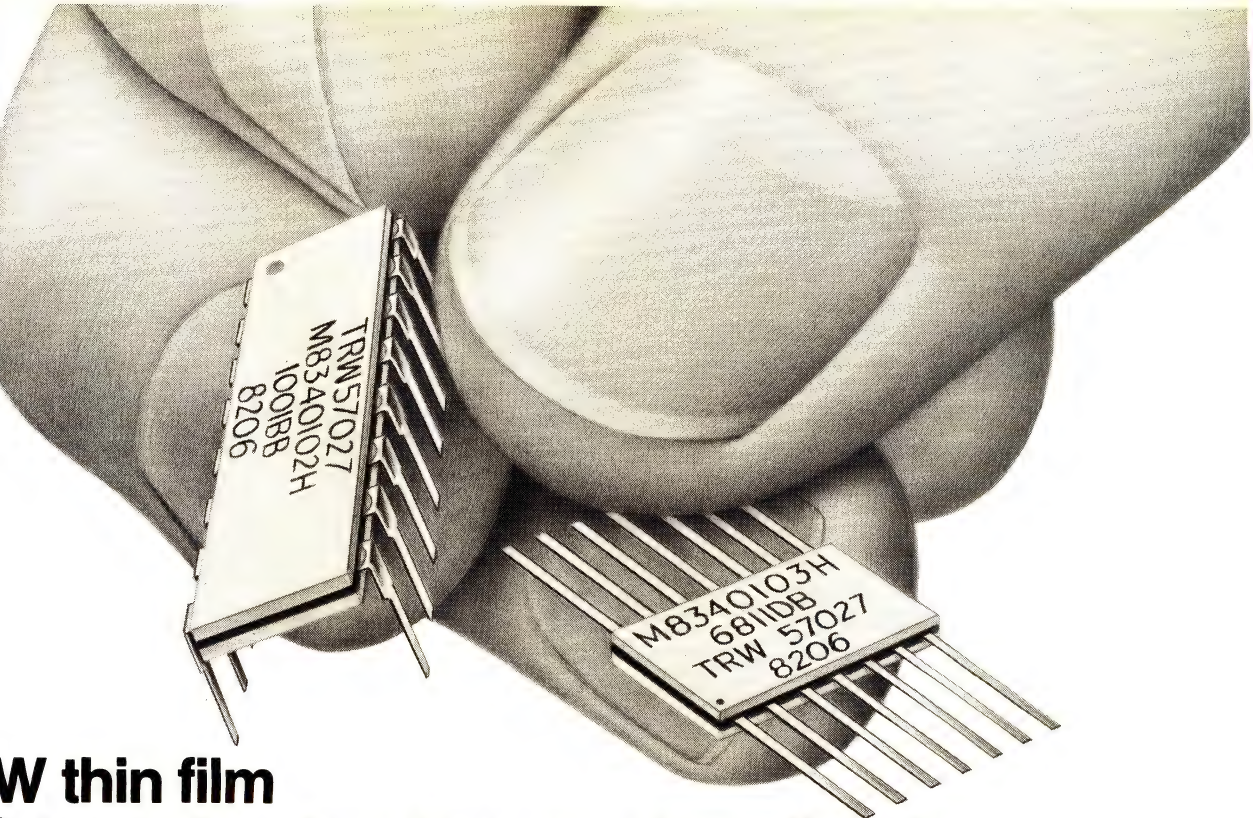

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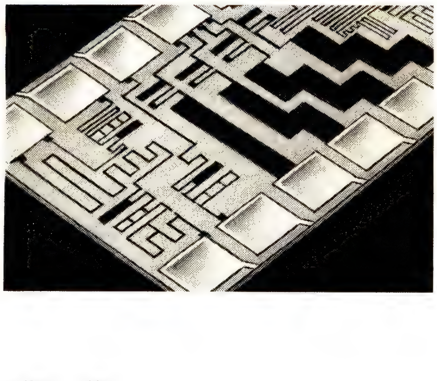

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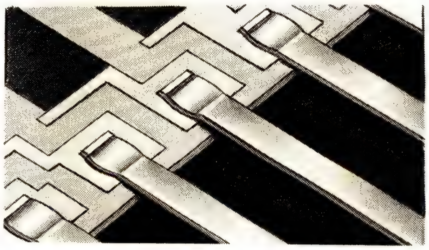

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International newsletter

Europeans get together on cellular-radio standard

Evidence is mounting that telecommunications-equipment manufacturers are about to get together on a European cellular-radio standard. The first sign was the recent joint response of Germany's Siemens, the Netherlands' Philips, and France's CIT-Alcatel and Thomson-CSF to a call by the French and German governments for bids to furnish a 900-MHz cellular-radio system for the two countries. **The system, EC 900, represents a compromise between Siemens' C-900 scheme and the MATS-E system first proposed by Philips and CIT-Alcatel.** Officials at Italtel, Italy's government-controlled public-switching manufacturer, now say that in order to promote a European standard, Italy will go along with the one chosen for the French-German project. Left out would be the UK, which has already chosen the U. S. Total Access Communication System (TACS) [*Electronics*, April 7, 1983, p. 102].

BT pilot project to link downtown London...

The centerpiece of British Telecom's efforts to make the City of London (London's financial district) a showcase of modern telecommunications technology—complete with satellite and broadband fiber-optic links—will be a trial run of an integrated services digital network (ISDN) linking 500 user sites. The net will be based on a System X digital local exchange, linked to 23 other exchanges, scheduled to go on line in the fourth quarter of 1984. Aside from testing the technology, **the ISDN experiment will be used to test the market for broadband data services,** such as teletex, basically a super-telex service; high-speed digital facsimile, which can transmit letter-size documents in 10 s; Photovideotex, an advanced Prestel service that delivers high-quality color photographs and text from remote data bases; videoconferencing; and other high-speed data services. BT plans to offer a national service in late 1985, and by fall 1986, its ISDN service will be available from 400 business centers served by a digital overlay network.

...using an intermediate ISDN

Rather than wait for the 144-kilobit/s standard from the International Consultative Committee for Telegraphy and Telephony (CCITT)—a standard that is still being formulated—British Telecom will kick off with an intermediate capability that pipes data into the office at 80 kb/s over a standard two-wire connection. The "standard," which will be current for five years, comprises a 64-kb/s voice or data channel, an 8-kb/s data channel, and a further 8 kb/s for signaling. Meanwhile, **wide-bandwidth users will have a dedicated four-wire connection at 2 megabits/s.** The idea is to link private automated branch exchanges directly. To allow different manufacturers' kits to talk, BT has therefore defined a new interface standard, called DPNSS, for Digital PABX Network Signaling System. Already, five local suppliers have endorsed the new standard, which will be enhanced later on to conform with any future CCITT standard for ISDN.

Esprit is first test of OSI protocol

Twelve European manufacturers of data-processing equipment recently agreed to adopt the International Standards Organization's Open Systems Interconnection (OSI) model as a way of opening up the formerly segmented European market [*Electronics*, March 22, p. 63]. **The OSI will get its first trial in a local network to be supplied to the Europe-**

an Community's Task Force for Information Technology and Telecommunications, in Brussels. Over the course of the next two years, Bull, ICL, Siemens, and Olivetti will be implementing the project, whose main goal is to provide communications between the task force and the participants in Esprit, the European Strategic Programme for Research and Development in Information Technology [*Electronics,* Jan. 12, p. 88], as well as to act as a public showcase for the benefit of potential users of the new protocol.

West German market for data processing sees boom time

West Germany's data-processing market is booming as it seldom has before. Indeed, thanks to slow shipments of semiconductor devices, some producers are having trouble filling orders. That is the gist of an analysis from Diebold Deutschland GmbH, the Frankfurt subsidiary of the U. S. computer-consulting and market research firm. For the first half of this year, Diebold predicts that (depending on size), incoming orders for computers priced at more than $100,000 will be from 10% to 25% higher than they were last year. For machines in the $10,000-to-$100,000 range, the firm forecasts a rise in orders of up to 30%. **The fastest-growing sector, though, is the one for microcomputers that sell for less than $10,000:** orders for these machines will rise from 35% to 70%, with the smaller systems scoring the biggest gains. For standard software, Diebold expects an increase of up to 50%. Behind the push, says the company, is a growing tendency to invest and—after several quite slow years—to satisfy pent-up demand. Other factors are the trend to equip office work stations with terminals that tie them to computers, as well as the need to enlarge data banks.

Honeywell adds Philippines to its Asian operations

Honeywell Information Systems Inc. has entered the Philippine market by appointing Distributed Processing Systems Inc., Manila, as its local distributor. Southeast Asia managing director Graham Moore says that Honeywell jumped in—despite a local financial crisis [*Electronics* March 8, p. 88]—for two reasons: to have a strong position when the economy picks up and to tie the Philippine operations into the company's existing network of Southeast Asian distributors. The regional office, in Hong Kong, looks after nine countries in Asia, and **without the Philippines and its rapidly growing population of 50 million, there would be a large hole in Honeywell's network,** says Moore. The Philippine computer industry purchased $36 million worth of equipment last year, a solid market for Honeywell, whose strength lies in its lines of superminicomputers and mainframes.

IBM links with Taiwan to aid development of computer products

IBM Corp. has contracted with the recently established New Development Corp. of Taiwan, which will handle research and development work on low-end computer products, including peripherals, for possible manufacture by IBM. NDC is a joint venture of the Industrial Technology Research Institute and the China Development Corp.—two organizations with close government connections. **The five-year contract is said to represent the first time IBM has assigned product development to an outside firm.** NDC is expected to have a staff of up to 100 specialists, joined by 8 technicians and 2 IBM executives.

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Transient analysis is a complex job: capture, digitizing, storage, display, analysis and data transfer. It's harder still if you need remote control capability. Most general purpose instruments can't handle more than one or two of these steps. But the Data 6000 Universal Waveform Analyzer does them all...with speed and power you won't find in any other single instrument. In fact, the Data 6000 offers more powerful capabilities than you could obtain from an entire roomful of equipment at many times the cost. Nothing else even comes close to the Data 6000, which offers you:

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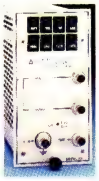
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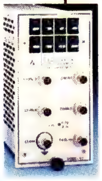
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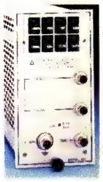
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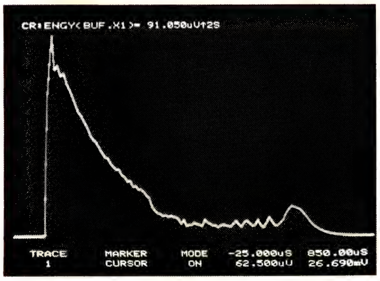

Compute and display a wide variety of functions from the captured signal. Useful functions for transient analysis are Rise, Fall, Settling, and Display Times; Overshoot, Maximum, Minimum, Peak to Peak, Area or Energy under the curve; Real and Complex Magnitude Spectra; Real and Complex Log Magnitude Spectra; and many more...all available with a single keystroke!

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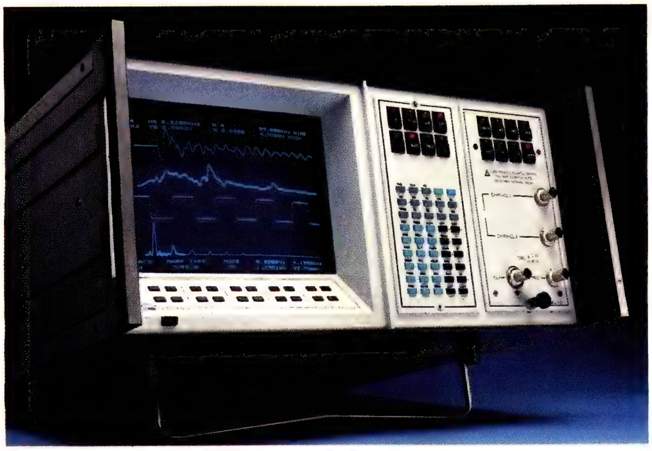

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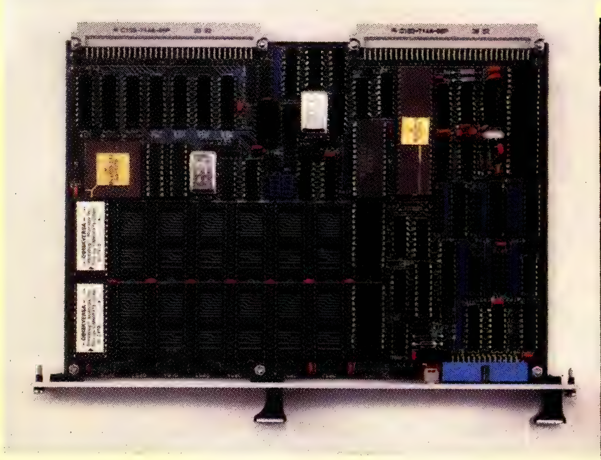
Motorola's 68000 MPUs – the commo systems from some of the industry'

Callan Data Systems uses the 68010 because "it's the fastest, most advanced microprocessor available."

"Motorola has established the 68000 product line as the **de facto** standard for the new generation of UNIX™ based super micro workstations and computer systems. Implementation of the chip on Callan's UNISTAR super micros is a perfect example.

"In the 16/32-bit UNIX-based microprocessor race, the 10 MHz virtual memory 68010 microprocessor, the heart of our UNISTAR 300 super micro, is the fastest, most advanced microprocessor available. It will remain one step ahead of the rest in the 16/32-bit UNIX microprocessor race."

Bill Pohlman, Vice President of Engineering, Callan Data Systems

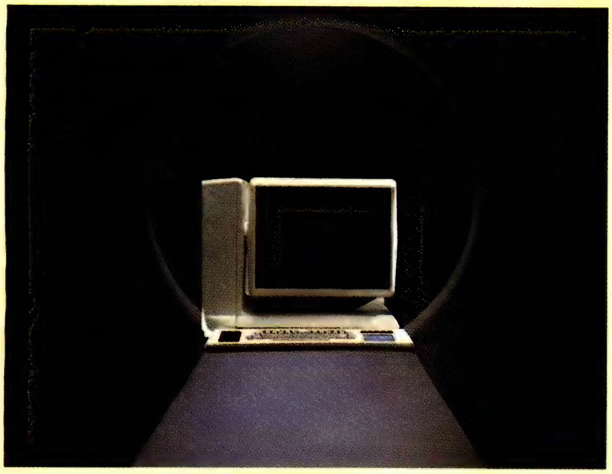


Omnibyte uses the 68000 in the single-board computer market for its proven reliability and quality.

"The single-board computer market that Omnibyte serves requires not only high performance, but also quality and proven reliability. For these reasons, Omnibyte chose the Motorola M68000 Family.

"The OB68K/VME1 incorporates the fast 12.5 MHz 68000R12. Its small-size, pin-grid array package allows room for more features on this sophisticated board-level computer."

Peter A. Czuchra, Marketing Manager, Omnibyte Corporation



Apollo Computer uses the MC68010 as the heart of its DOMAIN DN300 to deliver mainframe-like CAD/CAE functions in a desktop unit.

"Apollo's DOMAIN (Distributed Operating Multi-Access Interactive Network) is a high-performance local area network of dedicated computers operating in a distributed environment.

"The MC68010 microprocessor allows each Apollo DOMAIN to directly support virtual memory management in a network-wide demand paging environment. The performance and memory requirements of distributed CAD/CAE applications could only be satisfied with a design that incorporates microprocessors from the M68000 Family of devices.

Edward J. Zander, Vice President Marketing, Apollo Computer

The Sun Workstation® uses the MC68010 to achieve superminicomputer performance.

"The MC68010 is key to the architecture of our multipurpose technical workstations. We designed a special no-wait-state memory to take full advantage of the speed of the 68010.

"The 68010's symetric instruction set and virtual-memory capability are the foundations of a cost-effective implementation of UNIX. And UNIX is key to Sun's commitment to industry standards in hardware and software."

Lloyd Fugate, Vice President of Marketing, Sun Microsystems, Inc.™

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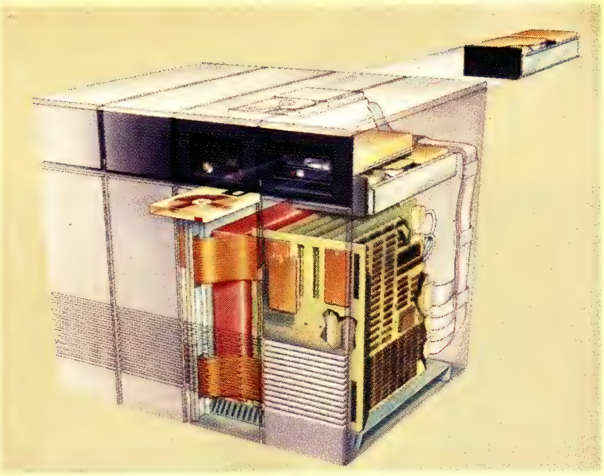


Convergent Technologies uses the 68010 as the heart of its MegaFrame system.

"The Motorola 68010, with its virtual memory, allowed us to build features typically found in mainframes and super-minis — features like demand page virtual memory — into our MegaFrame. So our MegaFrame is not a super-micro, it is a mini-computer, because of the 68010.

"Also, the 68010's linear address space is a real benefit for UNIX. We use up to 16 68010s in each system, all running on UNIX, all part of the 68000 architecture."

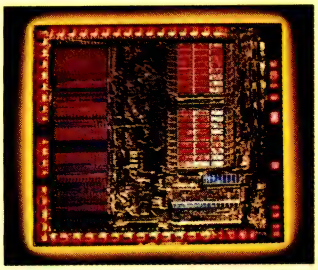
Steven Blank, Marketing Manager, Convergent Technologies

Intergraph uses the 68000 for improved screen response and more workstations per host.

"Creation of a screen image . . . is conducted up to three times faster than on a VAX-11/780.

"The MC68000 works with several Intergraph-designed processors to generate and manipulate graphic images locally . . . at the workstation. Offloaded of these burdens, the host computer is able to support many more workstations, such as executing database updates, running third party software and performing other background support tasks."

Bruce E. Imsand, Executive Technical Manager, Intergraph Corp.



Motorola's M68000 — the upward-compatible 8/16/32-bit microprocessor family — is today's common denominator for high performance systems.

Consider the overall cost/performance leadership of the M68000 Family and make your commitment. Your present and future generation products will be better for it. Get the inside story. Ask your design engineering management.

M68000: The upward-compatible 8/16/32-bit microprocessor family.

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The NuBus technology, designed at M.I.T., is optimized for 32-bit data and address transfers. Its 37.5-Mbyte/sec bandwidth combines with an elegant arbitration scheme to ensure fast and fair data flow.

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The NuBus design was developed to support sophisticated system architectures and eliminates the built-in obsolescence of processor-dependent systems. It lets you concentrate on developing applications, not architecture. Your significant investments are protected as new technologies develop.

The Nu Machine's open architecture solves your make vs. buy dilemma. Multiple-processor configuration support combines with the NuBus high bandwidth, high-resolution graphic displays, cache memory, and high-speed disks to make the Nu Machine system attractive to sophisticated end-users, systems integrators, and OEMs in the engineering and scientific marketplace.

Anticipating industry trends, the power and expandability of TI's Nu Machine allow it to accept 32-bit processors of the future.

Open system supporting industry standards

TI's Nu Machine system is currently available with a 10-MHz 68010 processor supporting a UNIX™-based operating system with enhancements for windowing and high-resolution displays.

Those who want to design their own system processors and controllers can now license the NuBus design from Texas Instruments.

Also, a NuBus-to-Multibus™ converter allows the use of existing interface cards and peripherals from third parties.

The system you can build on from now on

Because its high performance and flexibility are designed for the long run, TI's Nu Machine can be updated when other systems are outdated.

And, Nu Machine computers are backed by TI's service and customer-support network and by TI's commitment to quality and reliability.

To climb on the NuBus bandwagon, call toll-free: 1-800-527-3500. Or write Texas Instruments Incorporated, P.O. Box 402430, Dept. DNA203EC, Dallas, Texas 75240.

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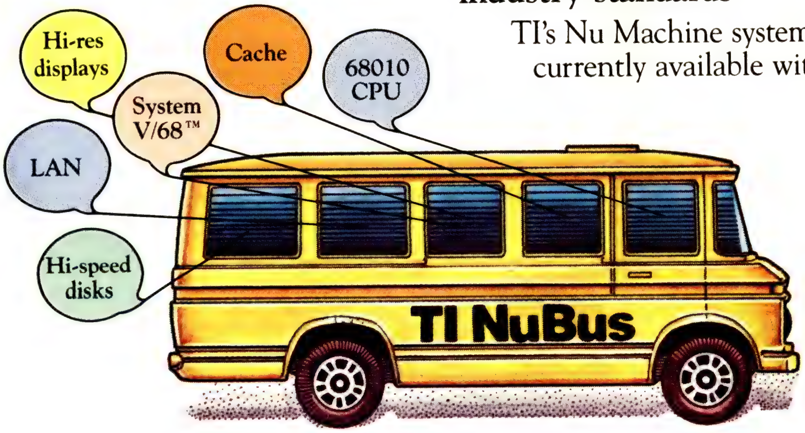

Combining innovative NuBus architecture with advanced graphics, powerful peripherals, and UNIX-based software, TI's Nu Machine provides the outstanding performance and flexibility required by scientific and engineering systems designers.

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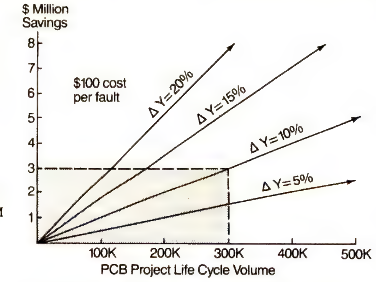
If you're going to build boards with technology like 8088's, 68000's, gate arrays, or custom VLSI, then you just can't test a better way. Thanks to a unique Teradyne invention called MultiMode,™ you'll get superior yields at system test.

MultiMode integrates in-circuit and functional testing in one system. It's just the item for complex VLSI designs. This capability lets the L200 generate yields on the order of 95% plus. An average greater by a full 10% than any competitive system.



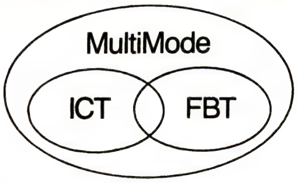
Increased yield is provided by higher fault coverage. And the savings are dramatic.

No tester does it better. And in a world where improving yields just 1% can mean savings of $1 million, it's a terrific advantage.

MultiMode Testing. Or 1+1=3.

By integrating in-circuit and functional testing,

MultiMode really is a case where the total is more than the sum of the parts.



Combining in-circuit and functional test techniques in one system. That's the secret of MultiMode.

This integration is what makes us so certain your yields will improve. MultiMode lets you apply both testing techniques in a single, comprehensive test program to find faults at the most effective level—device, cluster or board.

It's a strategy that stops faults from slipping through undetected. It's based on efficient programming, and on efficient diagnostics. Together making sure you get the highest levels of fault coverage as fast as possible.

And using MultiMode testing on a single powerful machine lowers work-in-process inventory build-ups around separate testers. Reduces board handling. And increases throughput.

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The L200 costs more than other testers out there. But it's worth it. Using MultiMode, your staff will get high fault coverage faster than ever before. And give you yields at system test that can save you millions.

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EXOS technology includes front-end processors for all Multibus,* VME bus, Unibus* and Q-Bus based computers and software supporting the standard TCP/IP high-level protocol. And if your host system supports any variety of UNIX,* then half a dozen network applications are provided as well.

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Avalanche diode extends glass-fiber transmission link

by John Gosch, Frankfurt bureau manager

Sensitivity is improved 7 decibels; gain is 10,000 at wavelengths between 1 and 1.6 micrometers

By redesigning the photodiode at the receiving end of a glass-fiber transmission link, researchers at Siemens AG have added another increment to the distance that a light-based signal can bridge between repeaters. Reiner Trommer and his team at the West German company's Central Research Laboratories, in Munich, have attained a 7-decibel improvement in receiver sensitivity, thereby extending the repeater-to-repeater distance by at least 5 kilometers. This for a link operating at wavelengths between 1 and 1.6 micrometers.

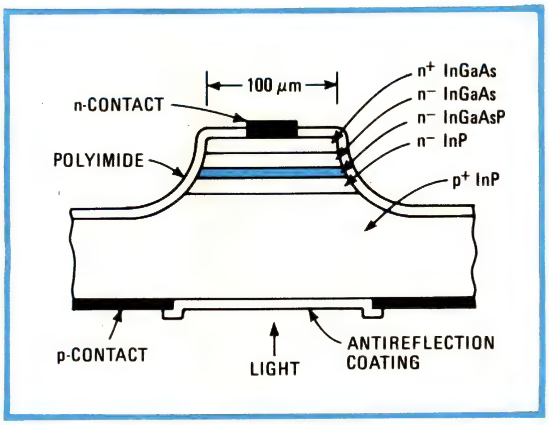
The researchers did it by using an indium gallium arsenide/indium phosphide avalanche photodiode with an intermediate InGaAsP layer. Equally important, they optimized the composition, the layer thickness, and the doping levels of the materials used.

The device is a mesa-type avalanche photodiode (see figure). The undoped 5-μm InGaAsP layer, a 3-μm InGaAs layer, and a tin-doped InGaAs contact layer are grown by liquid-phase epitaxy on top of a p-type InP substrate having a low density of dislocations.

One device sometimes used in long-wavelength optical receivers is the germanium avalanche photodiode. But although it has good internal amplification at high bit rates, it exhibits relatively large dark currents, resulting in high noise levels in a transmission system. An alternative, the InGaAs p-i-n photodiode, yields better sensitivities than germanium parts, at least for bit rates up to 500 megabits per second.

But these photodiodes make it difficult to obtain the avalanche effect necessary to achieve gain. For this reason, Trommer says, companies in the U. S., Japan, and West Germany are taking a hard look at InGaAs/InP avalanche diodes, which not only provide gain but have dark-current values low enough to produce only negligible noise in practical optical transmission applications.

Better value. Judging from the results published by other firms, Trommer believes that the avalanche photodiode his team has developed upstages competitive devices in several respects. For example, it achieves a maximum gain of around 10,000 in terms of the output current to primary photocurrent ratio, the result of optimizing the doping level and the thickness of the InP layer, where amplification takes place. At a gain factor above 10, the level at which the device is normally operated, it has a dark current of only 2 nanoamperes. This value, obtained by using high-quality InP and InGaAs epitaxial layers, is some 50 times lower than what other companies have reported so far, Trommer says.



Thin is in. The InGaAsP layer in this avalanche photodiode enhances speed by reducing the height of the barrier between the absorption and the multiplication layers.

As tests at the Siemens Communications group have shown, when the new photodiode is used in a 680-Mb-per-second optical transmission system, the low dark current translates into a receiver sensitivity of approximately 90 nanowatts, a value roughly 7 decibels better than can be obtained from p-i-n photodiodes, for example.

A 90-nW sensitivity is required for an optical system to produce only one error in 1 billion bits. It is because of this level of sensitivity that systems designers can space repeaters in an optical link farther apart.

Careful layering. The substrate, thinned to about 50 μm, has a doping concentration of 5×10^{18} per cubic centimeter. The thickness and the carrier concentration of the multiplication layer (in which amplification takes place) are precisely adjusted to achieve the high electric fields that are necessary for the avalanche process in the InP. The 3-μm InGaAs layer absorbs the light, and the 0.5-μm InGaAsP layer enhances the device's speed by reducing the height of the barrier between the absorption and the multiplication layers.

The diode is illuminated through the transparent substrate. The contacts—a gold-germanium n-contact on the top and a gold-zinc p-contact on the substrate—are evaporated and alloyed on the top layer and on the substrate. The active area on top, about 100 μm in diameter, is defined by mesa-etching in bromine diluted in acetic acid.

A polyimide photoresist protects the mesa edges, and a sputtered silicon nitride coating on the substrate's bottom prevents reflections. The device, which operates at 160 volts, could go into volume production within a year, Trommer says.

Trommer is now trying to develop this technology for integration into a preamplifier stage in an optoelectronic receiver. ☐

Software

Britain's fifth-generation-computer program aims to cut software-development costs

Alvey, Britain's fifth-generation-computer project, is up and running with a first contract to a consortium of UK companies that will develop better software tools for producing large real-time systems. Aspect, a $5.3-million project (the cost to be spread over three to four years), is aimed at applications in aerospace, industrial process control, and telecommunications (see "Has Alvey project fallen at first hurdle? Not at all," below).

In these areas, the time needed for software development can range from a few to many hundreds of man-years. Such projects are notoriously difficult to bring in on budget and within schedule.

Aspect grows out of work done by the project's head contractor, Systems Designers Ltd. (SDL), in Camberley, Surrey. In 1983, the firm introduced Perspective, one of the first integrated programming-support environments, currently used in two large European projects involving 10 sites in three countries. An enhanced version of Perspective, Aspect will provide tools to support all stages of software development, from the specification of requirements through design, programming, testing, and maintenance.

Multilingual. Aspect will provide all the usual programming aids, such as compilers and debuggers, for the development of embedded systems. From the start, it will support the Pascal, C, and Ada programming languages.

According to SDL's technical director, Geoffrey Holmes, the project's most important feature is that it will cook up software tools to control its overall progress. In the jargon of software developers, it will provide a project-support environment.

Holmes says the tools used in software development can process information about the software or the project. For instance, the compiler translates high-level languages directly into machine language. Design tools can model and check statements about the system's abstract design. "It is in the quality of this design and specification where major savings in implementation time and cost can be achieved," says Holmes. Other tools will provide project and version control, tracking the many changes made in system software before a design's completion.

Meanwhile, the project-support environment provides a common data store, or data base, for all information the tools use and does so in such an interconnected way that many functions are provided automatically. All the information in the project can therefore be provided automatically and kept consistent. The pro-

Has Alvey project fallen at first hurdle? Not at all

The Alvey fifth-generation project is to coordinate government, industry, and university research nationwide. Yet days after the Alvey directorate awarded a first contract, to a consortium of UK companies working on Aspect—an integrated project-support environment (PSE) for advanced real-time systems—a similar effort surfaced at British Telecom, which will team up with Imperial Software Technology Ltd., an independent software house set up to exploit the expertise of London's Imperial College. Over the next two years, British Telecom and its partner will develop a PSE that, like the Alvey project, will support telecommunications and other real-time projects.

At first, it looks like a case of reinventing the wheel, the thing Alvey was meant to avoid. Both systems will support the full software-product life cycle, from capture of user requirements to operational support and maintenance. Both are based on AT&T Bell Laboratories' Unix operating system, the use of which ensures portability to other host operating systems. Nonetheless, the emphasis of the two projects is different. Unlike previous initiatives in this area, British Telecom's PSE will be independent of high-level languages. The project's basis will be the Specification Definition Language, a graphical notation for capturing project descriptions. British Telecom believes that Vienna Definition Methods (VDM), first worked out by International Business Machines Corp. researchers some 10 years ago, can then automatically turn this description into high-level computer code. VDMs are mathematically based and can be used to write specifications that are scrupulously accurate.

Since both Aspect and British Telecom's PSE are supported by a common operating system, it will be possible to interchange software tools, particularly those that provide local and wide-area networking. In fact, informal discussions about this are already taking place between the two consortiums. It would be surprising if they were not: John Alvey, who headed the Alvey fifth-generation committee, is British Telecom's managing director for development and procurement.

–Kevin Smith

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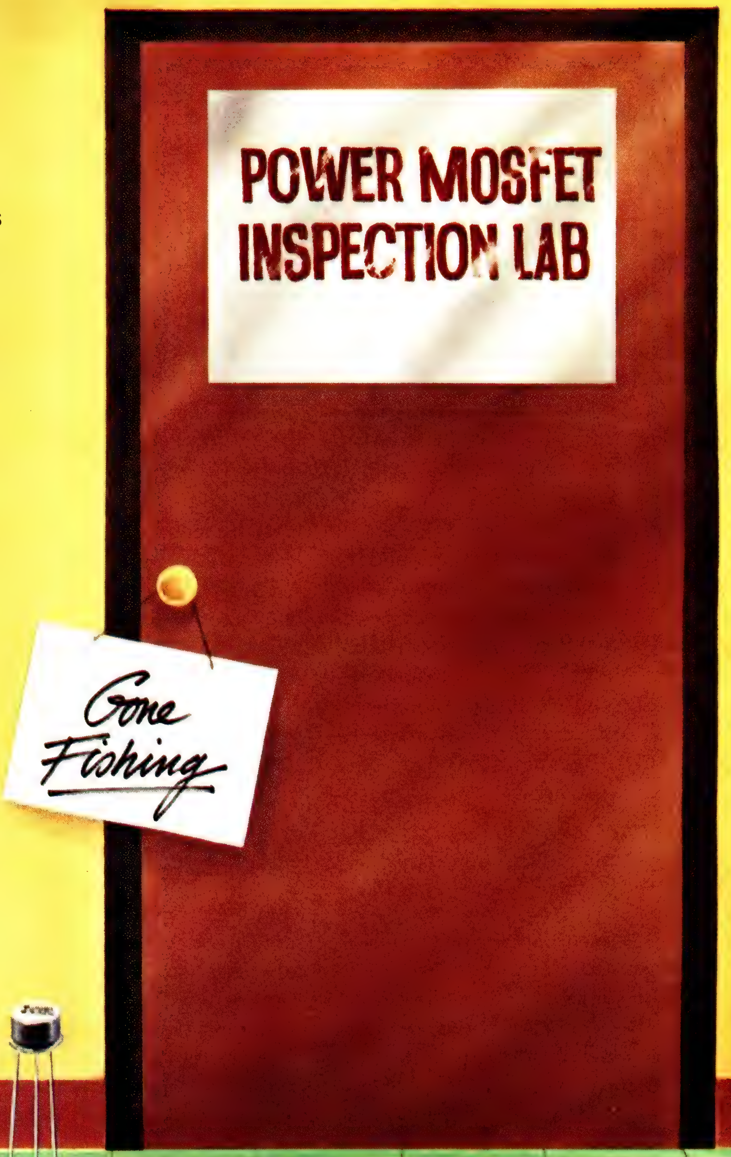

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ject-support environment can also give the productivity tools a single user-interface style.

Aspect's first release, in a year's time, will include these tools and standard utilities for AT&T Bell Laboratories' Unix operating system and will be hosted on the series 63 computers from GEC Computers Ltd. GEC will also be responsible for that series' basic software, which will subsequently be ported to other machines.

Under the Alvey project [*Electronics,* May 31, 1983, p. 101], several more advanced versions will be introduced. For example, a second-generation project-support environment will make it possible for software teams to be geographically distributed. A third-generation environment will probably support hardware development, too, and contain knowledge-based tools that can give software developers intelligent assistance. This third-generation environment is often referred to as an information-systems factory.

To add these facilities, SDL is collaborating with a consortium of UK companies, including International Computers Ltd. and MARI Advanced Microelectronics Ltd., as well as the universities of York and Newcastle. MARI is a small firm founded jointly by industry, the University of York, and the Tyne and Wear local government authority. ICL's contribution will be in the area of man-machine interfaces through Perq, its advanced single-user work station. ICL will develop the windowing software and the like necessary to support Aspect on Perq.

Goals to Newcastle. SDL will work with MARI to graft Newcastle University's Newcastle Connection [*Electronics,* Aug. 25, 1982, p. 64]—local-network software for systems that use Unix—onto Perspective. Thus connected, users can share computer resources and files transparently. Once in place, this facility will support teams of programmers geographically distributed at several sites and connected over local and wide-area networks.

The University of York's contribution is its Ada compiler. It will help to create a multilanguage working environment supporting Ada, Pascal, and C. Meanwhile, SDL will develop a public tool interface to help users self-tailor Aspect. **–Kevin Smith**

Telecommunications

U. S., Japanese jump into VAN lines

Japan's Telecommunication Business Act has just been submitted for expected Diet (parliament) approval and will not become law until next April 1. But even so, many U. S. and Japanese companies—which will be released from previously imposed severe restrictions—are rushing to get into enhanced services on data-processing networks, or value-added-nets.

The first announcement, by Fujitsu Ltd. president Takuma Yamamoto [*Electronics*, April 19, p. 75], revealed plans to open nationwide telecommunications services using leased lines in the first half of fiscal 1985, presumably right after the new law takes effect. Yamamoto said that he expected his company's VAN sales to reach $400 million by 1990.

AT&T International Japan Ltd. is reportedly negotiating with several potential customers, including the Industrial Bank of Japan and Mitsui & Co., who are interested in its Net 1000 data-transmission system. John W. Cusick, the company's managing director in Tokyo, would not comment on his marketing plans but said he was pleased with the compromise VAN act, which sets no limits to foreign participation in leased circuit networks and apparently simple procedures for registration and approval before opening a business. The original proposal, which drew heavy U. S. protests, placed a 33% limit on foreign ownership of leased-line nets.

"The new law looks very reasonable to us," he says, "and from discussions with Ministry of Posts and Telecommunications [MPT] officials, I am convinced that they are sincere in wanting to administer it fairly."

IBM-Japan Ltd. refuses, as usual, to comment on its plans, but company sources have been quoted as saying that the firm is preparing to announce its entry into the large-scale data-communications-network business. An IBM joint venture called Advanced Systems Technology—also involving Mitsubishi Corp. and Cosmos-80 Co., Tokyo, an IBM distributor—already has been set up to seek business in the emerging Information Network System, the $8 billion plan for a Japan-wide, all-digital communications network to be built during the next 15 years [*Electronics,* Aug. 25, 1983, p. 114].

NEC Corp. has also formed a new company—NEC Management Information Systems Ltd.—to develop in-house information networks, which may later be commercialized. Kyocera Corp., a major ceramics and fiber-optics firm, says it plans to operate a private services network between Tokyo and Osaka.

Legal suspense. Although the new VAN bill is more liberal than the original proposal, its outline remains hazy. The ordinances will not be written until after the Diet passes the basic legislation, later this summer, and could make the market-entry process relatively simple or grotesquely complex.

"They keep telling us that there will be no terrible surprises," says a U. S. Embassy official in Tokyo. "But bureaucratic ordinances are like land mines: you don't find out about them until you trip over them."

MPT officials claim that the law will not turn into a bureaucratic nightmare. "We are trying to do a 180° turnaround," says Norimasa Hasegawa, director of the International Affairs Division of MPT's Telecommunications Policy Bureau. "This is, after all, a grand experiment. That is why we are reserving the right to review the law after three years. Nobody really knows how this market is going to develop. I think it will be 10 years before we have a law which will be appropriate to the VAN market."

Another reason for Japanese caution has been a general fear, bordering on paranoia, that IBM's software power may enable it to dominate the

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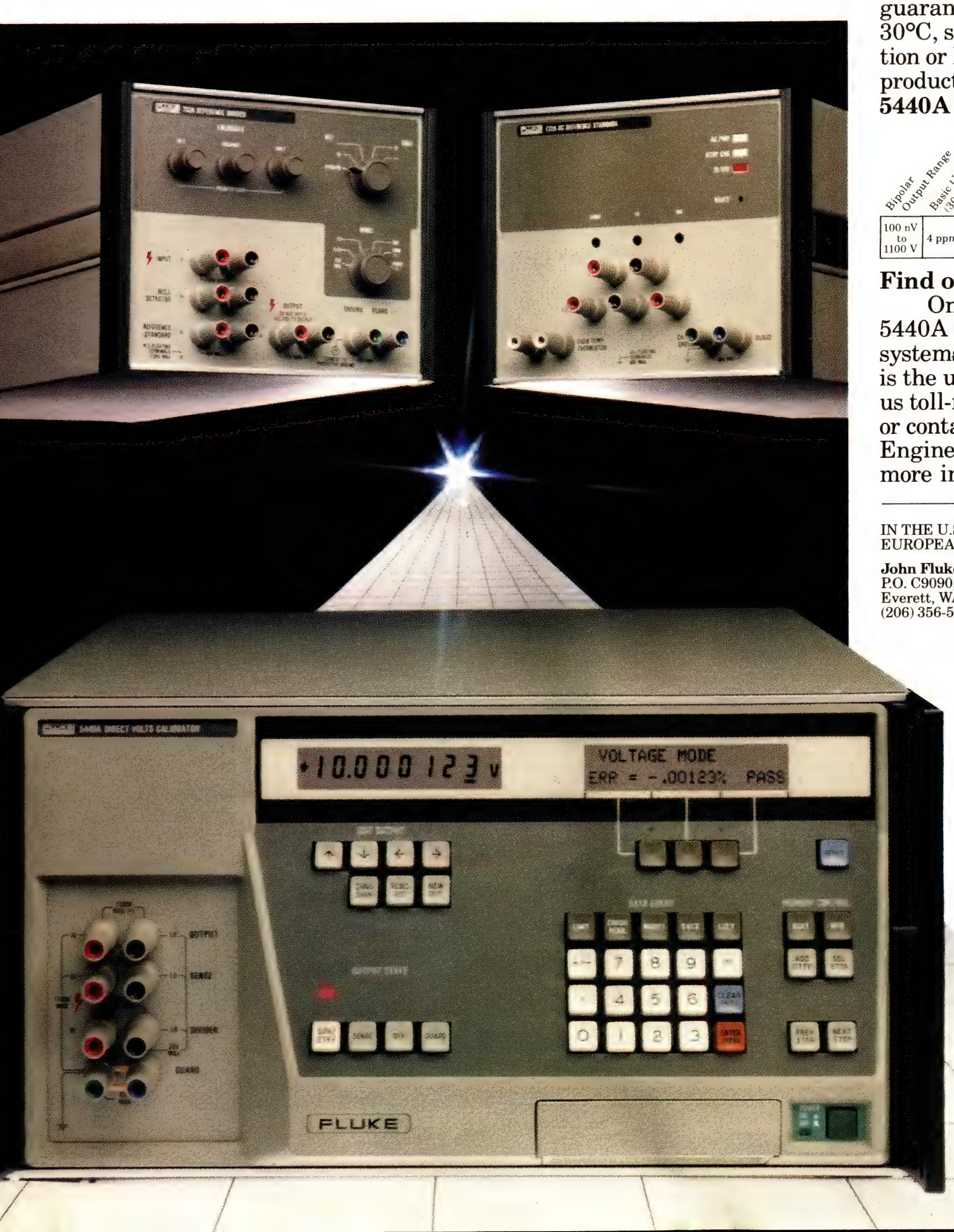

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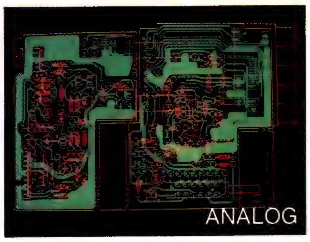

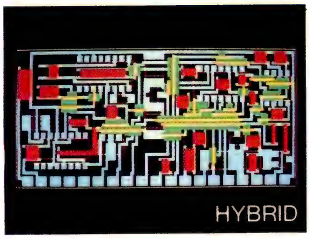

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market. This, say knowledgeable computer-industry people in Tokyo, is not likely to happen; nor is AT&T likely to dominate.

Says one U. S. executive: "IBM has tremendous computer expertise but communications is not a strong point. AT&T is tremendous in communications but not in computers. But that's the mix it takes to be a success in enhanced services."

More important to most U. S. companies in Japan is whether a companion law to change NTT from a public to a private corporation will allow the utility to use its telephone revenues to subsidize other activities, including VANs. If so, it will draw another round of strong foreign protests. **–Michael Berger**

McGraw-Hill World News

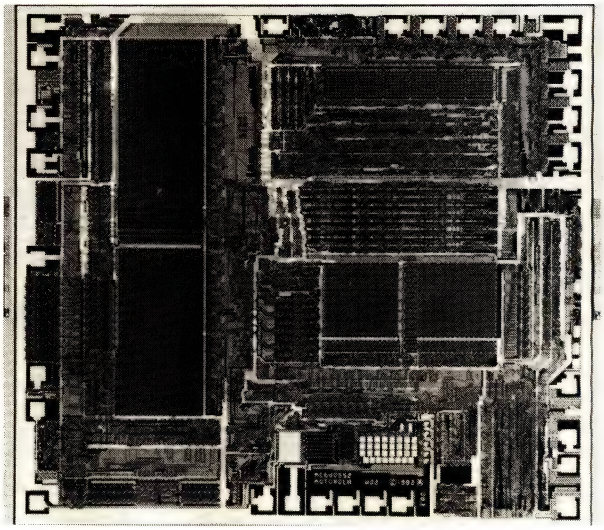
Solid state

Processor family builds from 6805

About to launch a major assault on the high-volume processor market, Motorola Inc. is designing a series of variations on its most successful 8-bit theme. The new effort will feature a higher degree of integration, with peripheral circuitry newly integrated on chip.

The Motorola effort will be spearheaded by two new microprocessors—the first of many to follow—built around the 6805 core just out of design. They were developed by a team led by Arturo Krüger, vice president of Motorola's European Semiconductor Division and director of its European design activities, at Geneva, Switzerland. The center has recently been designated the principal facility for designs related to the 6805 microprocessor.

Popular processor. The 6805 is a logical choice for the strategy because its already wide distribution means that equipment designers are generally familiar with its instruction set. In addition, Motorola has been producing so many of the processors for so long that it is well down the learning curve and can count on very high yields—an essential condition for circuits meant for high-volume and low-cost applications.



Forerunner. This Motorola MC6805S2 chip will be the first microcontroller from the company to use its serial-parallel interface. The SPI circuitry is the block at the chip's top center. The 32 white squares on the upper center right form the capacitor network for the analog-to-digital converter.

The two processors have in common a serial peripheral interface (SPI), which was designed for this program. It provides users with what Motorola claims are software-selectable options and levels of programmability far beyond those currently available in relatively low-cost microprocessors. Anil Gercekci, the company's manager for n-channel MOS designs, says he cannot comment specifically on how 8-bit microprocessor programs from such obvious competitors as Intel and Zilog—who are expanding their 8080 and Z80 families, respectively—will develop, but says that to his knowledge, the SPI-based circuits are the only ones in their price range making use of synchronous serial ports.

"Most low-cost microcomputers contain asynchronous serial ports where a start bit initiates an internal clocking mechanism," he explains. "With that kind of arrangement, it is costly, in terms of silicon, to regenerate the clock, and there are a lot of peripheral chips driven by the external clock."

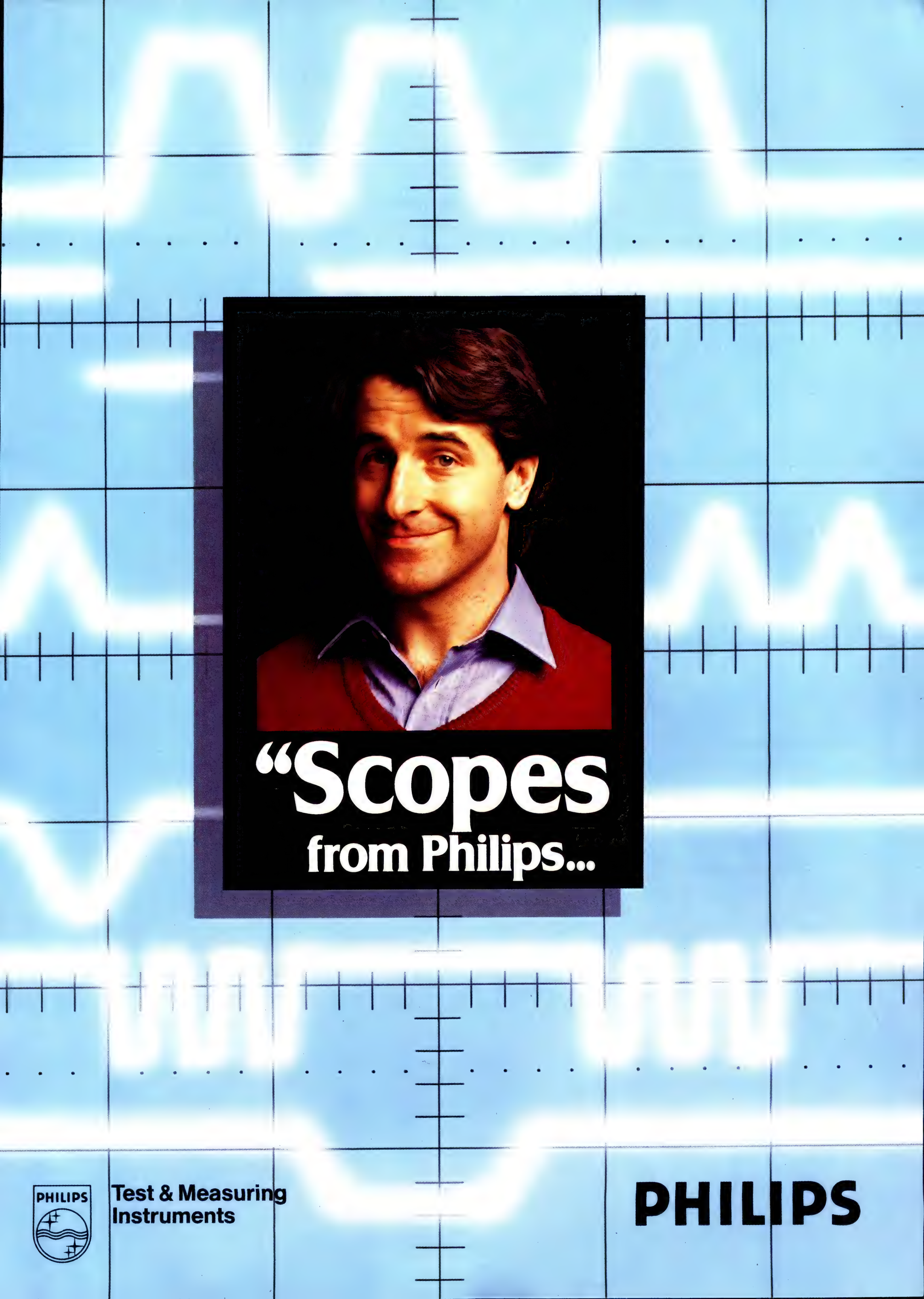
The advantage of Motorola's SPI, says Gercekci, is that it can be used in either data transfer or data reception and as clock master or slave, independently of which data mode it is operating in. What is more, the SPI takes only 6% of a chip's silicon, whereas generating that much flexibility with asynchronous serial ports might take as much as 15%, significantly raising components costs.

The SPI consists of an 8-bit shift register that may also be used as a data register for the integrated circuit; a divide-by-8 counter; slave-selection and arbitration logic; a control register; and start-and-stop-bit detection capability. Its clock line can be used as either master or slave, so that it can operate in a two-wire serial data-bus configuration or even in a multimaster environment.

EE-PROM coming. By the end of this year, Motorola will have put the SPI together with on-chip electrically erasable read-only memory. The company feels that the resulting microcontroller, the MC6805K2, has a bright future in a variety of fields. In automobiles, for example, its EE-PROM could be used as an odometer, or electronic key, while its 32 input/output lines could control displays.

Other potential applications would be in TV and radio tuning, with station information stored in the EE-PROM; keyboard control, with special characters in the EE-PROM; machine tools, with general sequences in ROM and execution sequence and parameters in the EE-PROM; and encryption, with key and modifiable algorithm in the EE-PROM.

Commenting on the new Motorola parts, William D. Mensch Jr., codesigner of the original 6502, says they might well attract users frustrated by the long waiting lists for the popular Intel 8048 and 8051 single-chips. **–Robert T. Gallagher**



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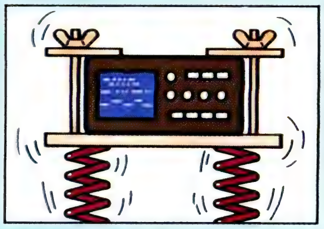
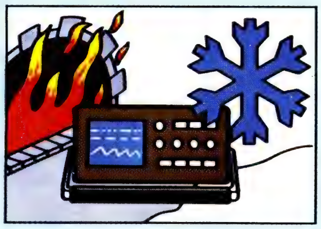
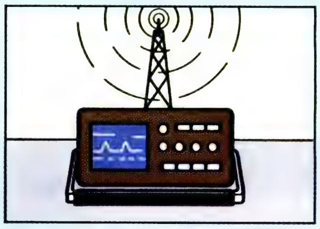


Tested with 30 g half-sinewave shocks of 11 ms. Vibration for 15 minutes in 3 directions at 5 to 55 Hz. Acceleration to 4 g.



Operates in a temperature range from – 10 °C to + 55 °C, allowing its use in the most demanding environments.



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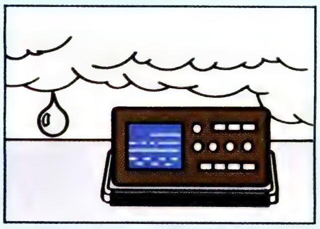

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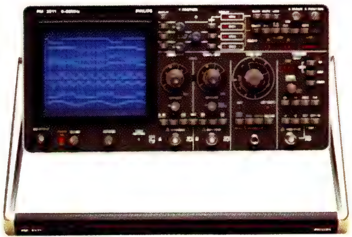

125 MHz Sampling rate – PM 3311
8 ns Single-shot resolution
200 ps Sequential sampling
4 Memories (total 1 K)
Post- and Pre-triggering (+ 9999 and – 9 div)
60 MHz Vertical bandwidth

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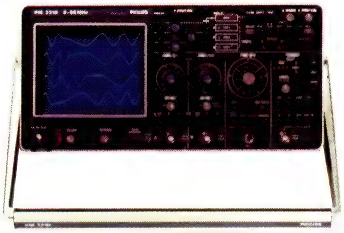

50 MHz Sampling rate – PM 3310
20 ns Single-shot resolution
200 ps Sequential sampling
4 Memories (total 1 K)
Post- and Pre-triggering (+ 9999 and – 9 div)
60 MHz Vertical bandwidth

CIRCLE NO 256

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Four channels – PM 3305
2 MHz Direct sampling
Sequential sampling to 35 MHz
4 K memory with compare mode
Pre-triggering 4 K
Dual-slope triggering
10 ns Glitch capture mode

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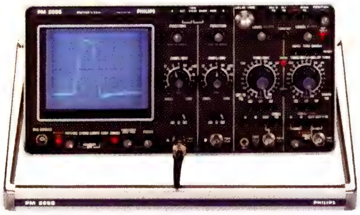
Analog



1000 div/μs Writing Speed – PM 3266
100 MHz Vertical bandwidth
Delayed sweep
Variable persistence
Third channel/trigger view

CIRCLE NO 255

24 h. "Baby Sitting" mode – PM 3219
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CIRCLE NO 257

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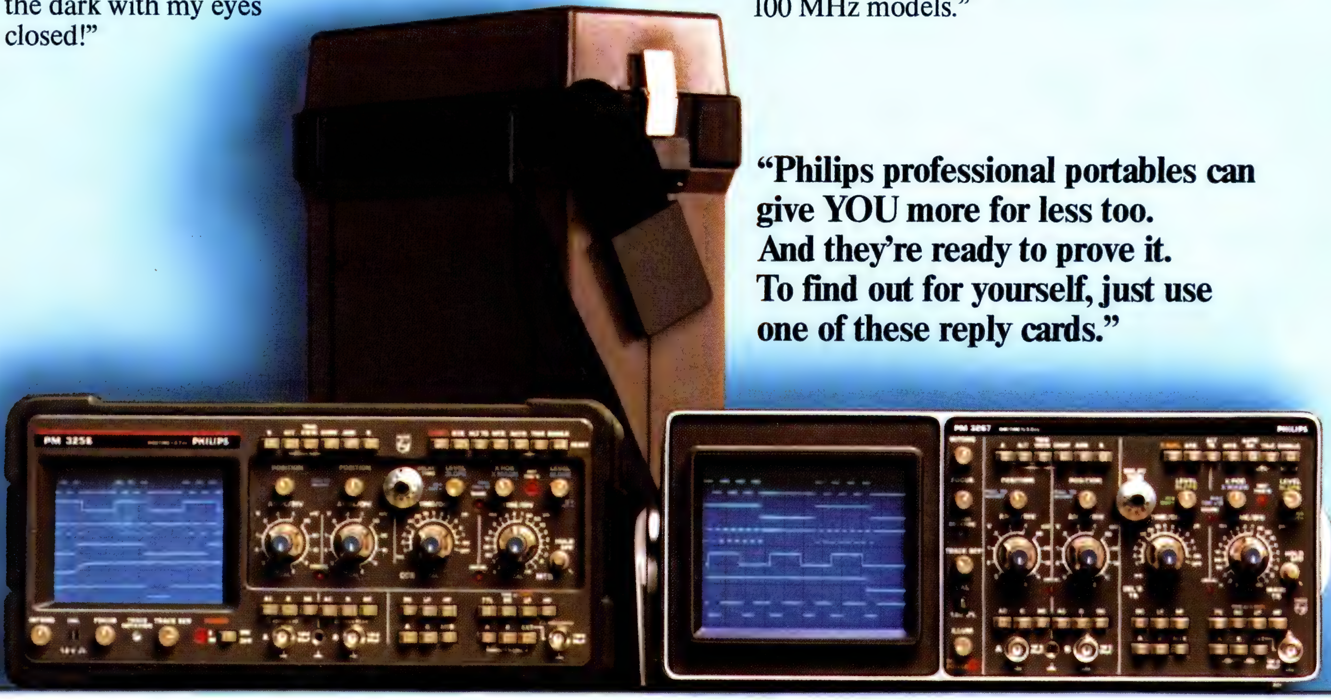

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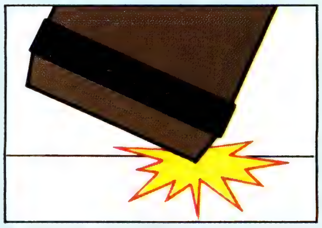
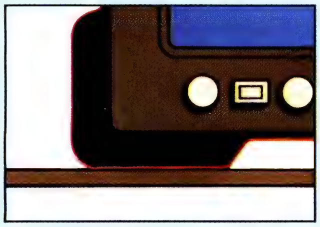
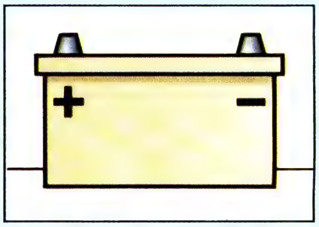
“Plus” benefits



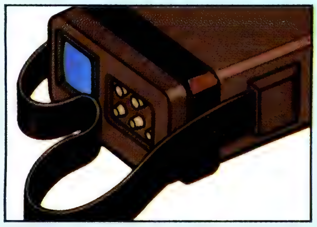
Rugged front-panel case protects Philips scopes from damage. Special clips latch cover.



Protective rubber bumpers on all corners protect the instrument from hard shocks in industrial environments.



Optional power by battery or other DC source gives each instrument extra versatility for a wide range of uses.



Handy carrying strap makes the Philips professional super portable extra-handy, even for use in the field.

Back home, Daewoo's Park makes a corporate contribution

When Sung Kyou Park left a comfortable job as a senior research engineer in the U. S. to return home to his native South Korea in 1978—"at less pay and twice the hours"—he was responding to a challenge and, he felt, a need. "I felt that I would be more important here than in America," says the 45-year-old executive vice president of Daewoo Telecom Co.

Park, who earned a degree in electrical engineering from Massachusetts Institute of Technology and his doctorate at the University of Texas, worked for five years at Schlumberger Ltd., before coming home. Time has proved his move a wise one. He was put immediately in charge of a subsidiary firm, and last year, when Daewoo reorganized its electronics operations and created the telecommunications company to handle all industrial products, Park was given the task of putting it together.

Now, using a wide-ranging technical agreement with Northern Telecom Ltd. that includes both technology and design, Park hopes to make Daewoo a leader in Korean electronics. Sales last year were a modest $33.8 million, but he projects that figure will more than double in 1984 and will continue doubling for at least five years.

Park is basing his growth strategy on an annual investment that amounts to 6% of Daewoo Telecom revenues into research and development. The staff at the R&D center in Inchon has grown from 24 to 150 in two years, and by year's end, it will total 180 researchers, many of them overseas returnees like Park. Their work will support Daewoo Telecom's activities in digital switches, optical-fiber systems, and semiconductor production.

Using licensed Northern Telecom technology, Daewoo Telecom is producing the Canadian firm's S-1 digital switch for domestic and overseas sales. Local content goals, Park said, have been accelerated by a full year, meaning that 65% of the switch is now made in Korea.

Home again. Sung Kyou Park left a comfortable job as a senior research engineer in the U. S. to return to his native South Korea because "I felt that I would be more important here than in America."

The company has a semiconductor pilot plant in operation, but a final marketing decision, he says, has not been made. "If we go into memory, "my recommendation will be to skip the 64-K dynamic RAM and go directly into 256-K production.

"But the custom and semicustom chip market share will grow to perhaps 40% by 1986. I think that market makes more sense for us." In fact, Daewoo Telecom has opened a subsidiary called ID Focus in Sunnyvale, Calif., to develop custom designs for in-house use and to seek American business.

LEP has a social role, too, says managing director Hurault

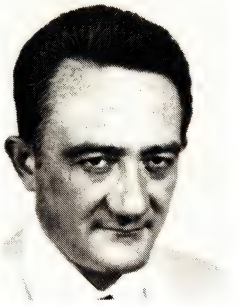
For Jean-Paul Hurault, the Laboratories d'Electronique et de Physique Appliquée is more than just a research institution. True, under that unassuming name, LEP is responsible for the development of future technology in a number of strategic areas for Philips, the mammoth Dutch-based multinational conglomerate.

But Hurault, recently appointed managing director of the laboratory—located in the Paris suburb of Limeil-Brévannes—feels that LEP's role is also highly social. "We really have a double mission," he explains. "It consists first in preparing for the medium- and long-term future, from about two to five years hence, for the French industrial companies with which we are associated, like RTC-La Radio Technique Compélec and TRT.

"But we also have a social responsibility, and that's the creation of employment. What our research should be doing is to lead to development and, finally, production that will mean new jobs."

Hurault, 43, is a graduate of the prestigious Ecole Polytechnique and joined LEP in 1970 to head up basic research. After a stint in Eindhoven, the Netherlands, as part of the Philips Research Coordinating Committee, he returned to LEP in 1977 as director of telecommunications research and, after a year, was made deputy managing director.

A specialist in solid-state physics, Hurault is very much in his element at LEP, which is designated the principal Philips laboratory for research in gallium arsenide microelectronics. The GaAs research team has already scored a number of world firsts, the most recent being a one-chip receiver for television signals from direct-broadcast satellites [*Electronics*, March 8, p. 81].


Conscientious. Jean-Paul Hurault feels that LEP has a responsibility to society.

LEP has some 350 people, part of the surprisingly large total of 30,000 employed by Philips in France. Those employees represent nearly 10% of the worldwide total, yet the firm maintains a resolutely low profile in France. Principal research work for the lab includes photodetection and TV circuitry, medical systems, radio links, and software development. ☐

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DIVISIONE COMPONENTI

Circle 136 on reader service card

With add-in modules, 24-channel analyzer grows to suit needs

by John Gosch, Frankfurt bureau manager

Basic 24-MHz analyzer can be configured with faster cards; other boards add software mapping and protocol analysis

If a relative newcomer in the crowded field of logic analyzers wants to make an impression, it had better have something special up its sleeve. Rohde & Schwarz thinks it has that something in its logic-analysis system, the LAS. Its predecessors relied heavily on outside technology, but the LAS is a true R&S in-house design.

The 24-channel instrument—expandable to 96 channels—emphasizes modularity and a built-in generator. Its options include the latest measuring methods, such as event-timing analysis, Basic-language processing display, software mapping, and protocol analysis.

Further, the LAS sports an analog recorder, so that users can handle not only digital but also hybrid (digital and analog) systems. It also boasts a selector that picks out word sequences and data combinations in addition to individual words.

Together with the intelligence afforded by the built-in 16-bit microprocessor, this feature set in a single instrument "sets new standards for processing and displaying analysis results," says product manager Peter Bernhard. Of note, too, is the instrument's wide range of applications, including performance analysis of programs, systems, and communications networks; functional analysis of process-control systems; in-service monitoring of digital equipment; protocol analysis in data-transmission systems; functional tests of digital circuits; hybrid testing; and automatic test runs (made possible by an integrated IEEE-488-bus controller).

Bernhard says the LAS, with a 20-MHz analyzer that can handle up to 72 channels simultaneously, is an efficient tool for optimizing any kind of program or system. Printed-circuit boards with 100-MHz analyzer sections and eight channels give the LAS its 96-channel capability.

Data selection. The analyzer stands out by virtue of its multilevel data-selection technique. Independently of the trigger facility, this selector function lets users pick out not only individual words but also word sequences, data types, and data combinations and ranges from the data stream. The selector replaces the conventional simple qualifier facility with eight sequential decision levels with random branching.

Thus the execution of, say, a microprocessor instruction can simultaneously be qualified as a whole, including the operating code, operand, and data-transfer cycle. Also, it is possible to choose segments from data-transfer protocols for analysis.

Bernhard says that all this makes it easier to handle such important measuring tasks as data compression in software-performance analysis, the selection of faulty data and of data packages, the systematic investigation of individual instruction types or partial functions, and the analysis of data-transfer protocols.

By handling logic events selectively, the event-timing display—the LAS-B5 option—marries the advantages of a conventional timing display, such as easy interpretation of timing relationships between pulses, to those of state display, such as easy interpretation of commands.

A diagram with a horizontal time

base represents the event timing. For that, the LAS uses a time-stamp facility (with a maximum resolution of 100 ns) that provides each logic event with a time marker and is the basis for event-timing display. Its 30-bit resolution allows display of long-term events at high resolution.

The processor option, LAS-B4, includes a computer running under the CP/M-86 operating system, a real-time clock, and dot-matrix graphics. Basic-language programs can process all data directly. This translates into free programming of any display and such evaluation modes as histogram display of time and frequency distribution, mapping of program activities, and analog display of digitally coded control parameters.

100-MHz channels. For high-frequency timing, the LAS has high-speed channels and an option, LAS-B1, with eight channels at a 100-MHz sampling rate. Expansion to 16 or 24 channels is possible with the LAS-B2 option, an additional eight-channel board. The 100-MHz analyzer works with its own trigger facility or in the master-slave mode, in conjunction with the state analyzer.

Two logic-generator options, the LAS-B6 and -B7, produce digital test patterns with a 20-MHz clock frequency. An analog-recorder option, the LAS-B9, analyzes hybrid circuits and is suited to process control.

For all the setup and evaluation possibilities created by the LAS, it is easy to operate. Soft keys that have proven themselves on other R&S systems reduce instrument handling to a minimum and guide the user so adroitly that errors are all but eliminated. The soft-key operation automatically adapts itself to measuring options and coordinates the interplay of simultaneously run options.

The instrument works by means of programs (in the 16-bit microprocessor) that configure themselves to the measuring option at hand.

In a basic configuration, with 24 channels sampling at 20 MHz, the LAS sells for roughly 26,500 DM on the German market. Delivery takes about four weeks.

Rohde & Schwarz, P. O. Box 801469, D-8000 Munich 80, West Germany [Circle reader service number 441]

GaAs-based communications links provide outlying areas with radio and video signals

France is famous for wine, food, and impenetrable bureaucracy. Sodielec, a small company at Millau, a region whose reputation rests on the first two, has just fought and defeated the third. Now the firm has the right to take to market what it regards as a unique product: a compact, lightweight radio link that brings reasonably priced communications to places the national network cannot reach.

Sodielec (Société de Diffusion pour l'Electronique) had to convince the French postal and telecommunications authority that the system did not encroach on the government's domestic telecommunications monopoly. After four months of what the company calls "a great deal of perseverance and doggedness," it was awarded the PTT sanction that allows it to sell the system in France.

Up to 30 GHz. This Ranal system is available in two versions: SFH 120, for standard telephone-type communications, and SFH 300, for video transmission. Like the SFH 300, the SFH 120 is a complete duplex link based on gallium arsenide field-effect transistors. It can operate from 9 to 30 GHz, though it is particularly well adapted to the 23.5-GHz standard for European light-radio-link communications.

GaAs technology helps each terminal in the link fit into a cylindrical package only 27 cm in diameter by 23 cm deep and weighing just 4.5 kg, antenna included. With a power consumption of less than 1 W, the link can run off batteries, solar panels, or any other source than can furnish its 11-to-15-V supply.

Directly connectable to a switched network, the SFH 120 will no doubt find its commonest applications in rural telephony. Sodielec anticipates many other uses, from remote measurement and control to data transmission. The company expects the links to be used at airports and seaports, construction sites, stadiums, and exhibitions, as well as in rescue work. In fact, the links have an edge on the standard communications infrastructure in just about any application that demands ease of installation, a byproduct of their small size and low power consumption. The average transmission range is 10 km.

Triple-header. Capable of handling color-video and high-speed data transmission, as well as digital multiplexing, the SFH 300 is a more complex system, about as small as the SFH 120 at more or less double the power consumption. Users can choose between color-TV transmission in any of the three international standards—PLA, SECAM, or NTSC—or opt for broadband remote control for measurement or data transmission at the European standard of 2 Mb/s. Besides images or data, an auxiliary channel permits the simultaneous transmission of sound and, say, remote-control or remote-measurement data.

Sodielec expects that the SFH 300 will be used primarily in applications that call for remote TV cameras. Other possibilities are related to TV signal reception from direct broadcast satellites. The unit's average range is about half the SFH 120's.

Both the SFH 120 and the SFH 300 will be available by June for about $2,200 and $3,500 a pair, respectively. In addition, Sodielec will

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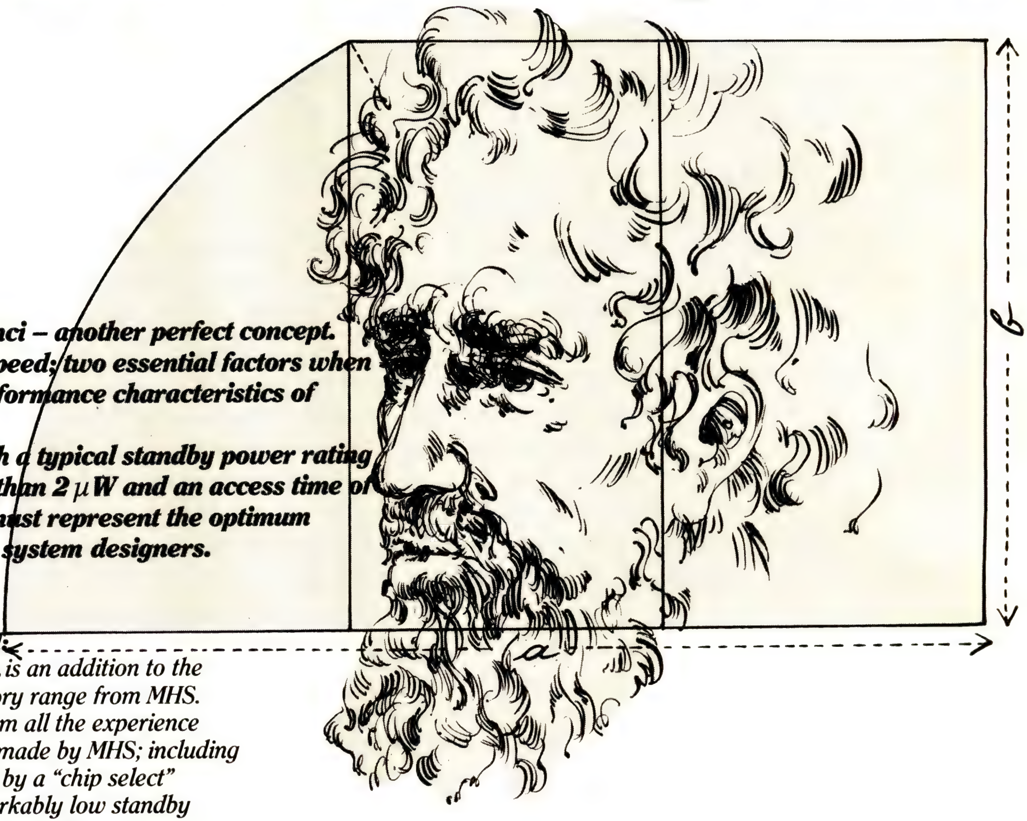
HE HM 65261: sheer genius



Four centuries after de Vinci – another perfect concept.

Power rating and speed; two essential factors when considering the performance characteristics of memory devices.

The HM 65261, with a typical standby power rating (25 °C, 2 V) of less than 2 µW and an access time of 60, 70 and 85 ns, must represent the optimum solution for today's system designers.

Its background:

The 16K x 1, HM 65261, is an addition to the 16K CMOS static memory range from MHS. This device benefits from all the experience and key achievements made by MHS; including input gating controlled by a "chip select" feature providing remarkably low standby currents. Moreover, the flexibility of the x 1 format is ideal for all applications calling for parity or error correction "bits".

Military version approved

Totally reliable across an operating temperature range of – 55 °C to + 125 °C, the HM 65261 is especially designed for military applications demanding high levels of circuit integration, but still able to serve industrial requirements.

MHS: a leading European supply

Just 12 months after the launch of the 2K x 8 CMOS static RAM (HM 65161), one of the fastest of its kind, MHS has continued this development with the advent of the HM 65261 – designed, developed and manufactured at its Electronic Centre in Nantes.

Here, at last, is the European CMOS source System Designers have been waiting for.

HM 65261	*0 to 70 °C*	*– 55 °C to + 125 °C*
Access Time Taa	*60*/70/85 ns*	*75*/85/100 ns*
Standby current ICCSB1 *CS = VCC-03 V*	*50 µA*	*900 µA*
Standby current ICCSB *CS = VIH* *Input gating*	*3 mA*	*4 mA*
Operating Supply Current ICCOP	*50 mA*	*50 mA*
Package 20 pin	*Plastic, Ceramic, LCC*	

**Introduction june 1984.*

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Circle 137 on reader service card

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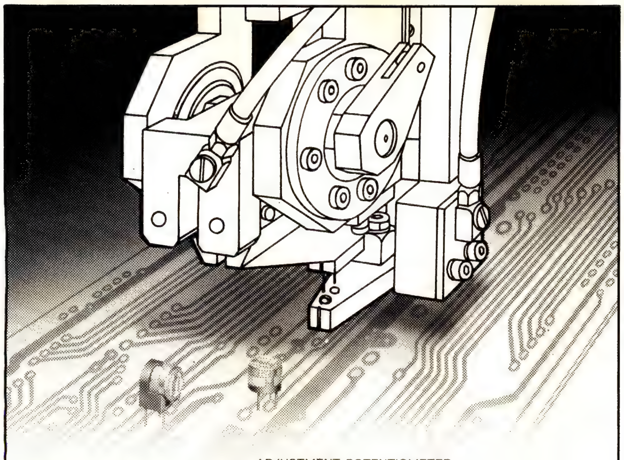

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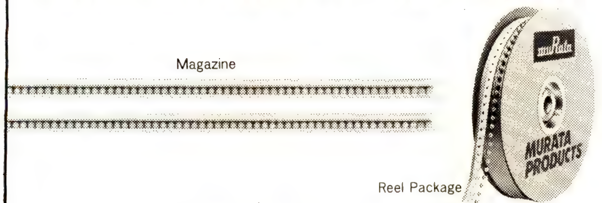

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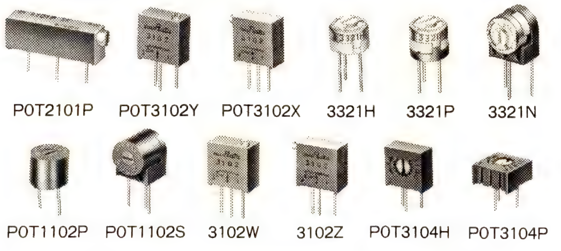

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Circle 138 on reader service card

market each in an export version, which will use parabolic antennas and achieve significantly more powerful ranges by transmitting in the 10-to-15-GHz band. Prices are about 10% to 20% higher than those of the European versions.

Sodielec, Saint-Georges-de-Luzençon,
12100 Millau, France [Circle 442]

Low-cost terminal offers 1,024-by-780-pixel resolution

Offering a 1,024-by-780-pixel resolution on a 14-in. screen, the D-Scan GR-1104 color graphics-display terminal is available for £4,250 upward in single-unit quantities. That is considerably less what than other standard-size graphics terminals cost.

The GR-1104 has a 60-Hz noninterlaced refresh color display that generates natural images, an ergonomic keyboard for fatigue-free operation, and an ASCII character set with 94 characters. It can display 80 characters by 48 lines, and its character font uses 12-by-16 dots. In addition, the terminal has independent graphics- and character-screen structures that offer simple programming and editing and provide such flexible screen-manipulation capabilities as superimpose.

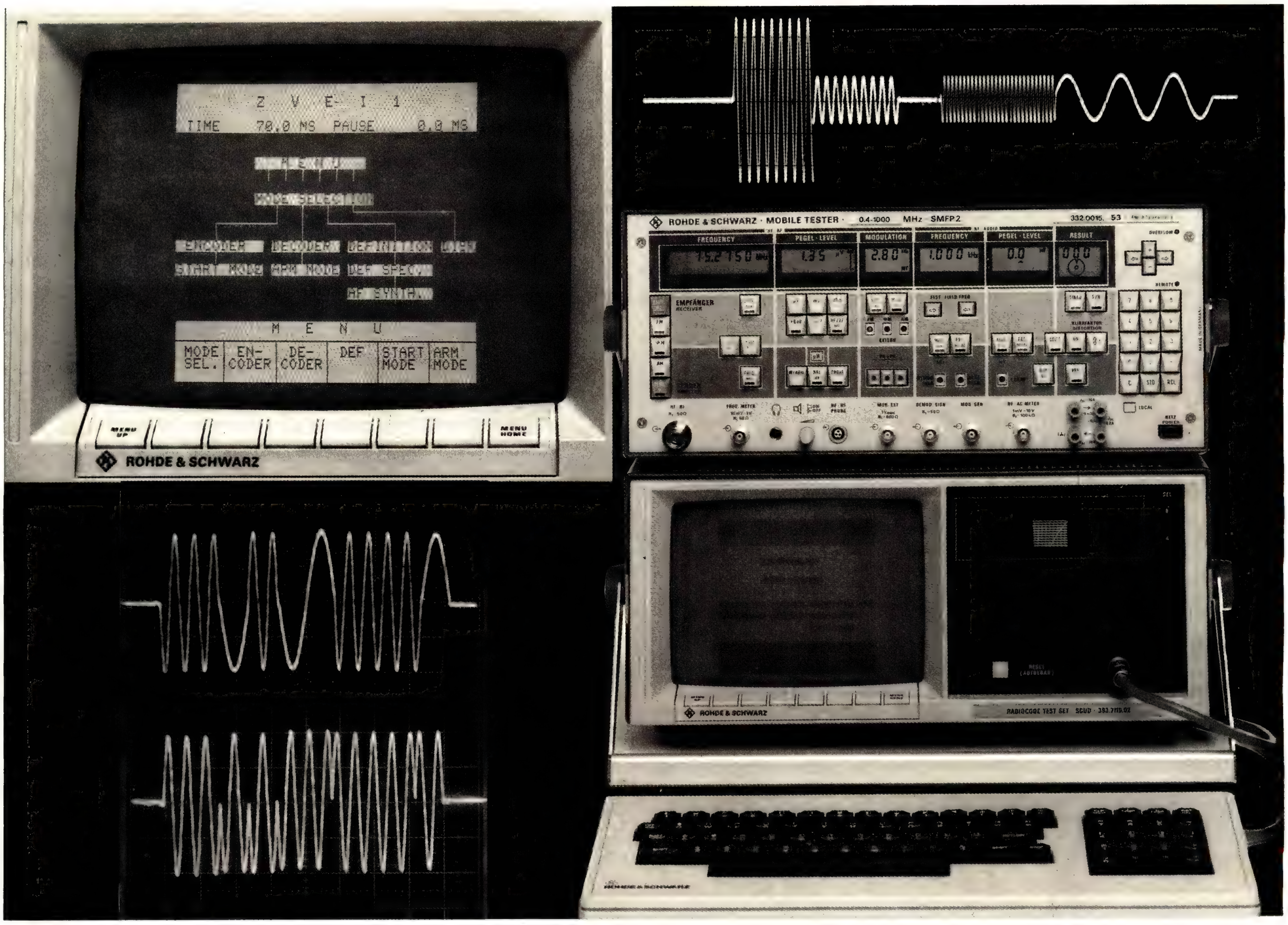
The GR-1104 is available with three separate high-resolution input/output tablets for a choice of reading areas: 307 by 204, 500 by 500, and 640 by 461 mm. A Tektronix 4010 series emulator lets users execute existing application programs for the 4010 series of graphics terminals.

Ambitron Ltd., 13 The Paddock Industrial
Estate, Hambridge Rd., Newbury, Berkshire
RG15 5TQ, England [Circle 444]

Regulators have voltage drop of only 0.4 V at 400 mA

The SGS LM2930A and LM2931A 5-V regulators resemble the LM2930 and the LM2931 but feature lower input-to-output voltage drops and higher current capabilities. Both de-

Radio voice and data — the complete measuring solution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M E N U
MODE SEL. EN-CODER DE-CODER DEF START MODE ARM MODE
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Circle 140 on reader service card

liver up to 400 mA; their voltage drops are typically 0.2 V at 150 mA and only 0.4 V at 400 mA.

The LM2930A includes protection against 40-V load dumps, negative transients, reverse polarity, and overvoltage; it also has foldback-current limiting and thermal shutdown. With load-dump protection rated at 60 V, the LM2931A has the same array of protection features as the LM2930A. Suitable for automotive applications, the LM2930A and LM2931A can supply their 5 V even during cold start-ups, when the battery voltage may fall below 6 V.

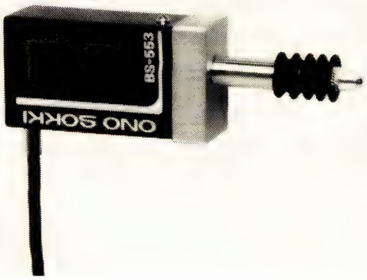
SGS Ates, Via C. Olivetti 2, 20041 Agrate Brianza, Italy [Circle 445]

Compact linear gauge sensor measures with high accuracy

The BS-553 linear gauge sensor features a 5-mm measurement range with 1-μm resolution and provides such features as a dustproof rubber boot. Packaged in a compact, lightweight case, it takes measurements inside machinery that until now could not house such sensors. The unit is ideal for mounting in locations where gauges cannot be viewed directly, in such moving devices as robots, and in dangerous locations.

In combination with a digital gauge counter, the BS-553 can take dimensional measurements with high accuracy. It has more than 30 times the shock resistance of conventional mechanical gauges. Many display units and recorders can enhance the BS-553's range of applications.

Ono Sokki Co., Shinjuku NS Building, 2-4-1 Nishi Shinjuku, Shinjuku-ku, Tokyo 160, Japan [Circle 446]



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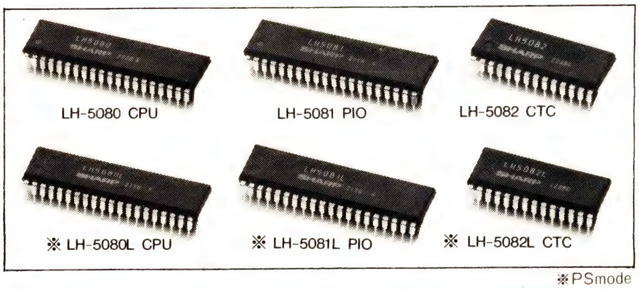

LH-5080 CPU LH-5081 PIO LH-5082 CTC

※ LH-5080L CPU ※ LH-5081L PIO ※ LH-5082L CTC

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Circle 97 on reader service card

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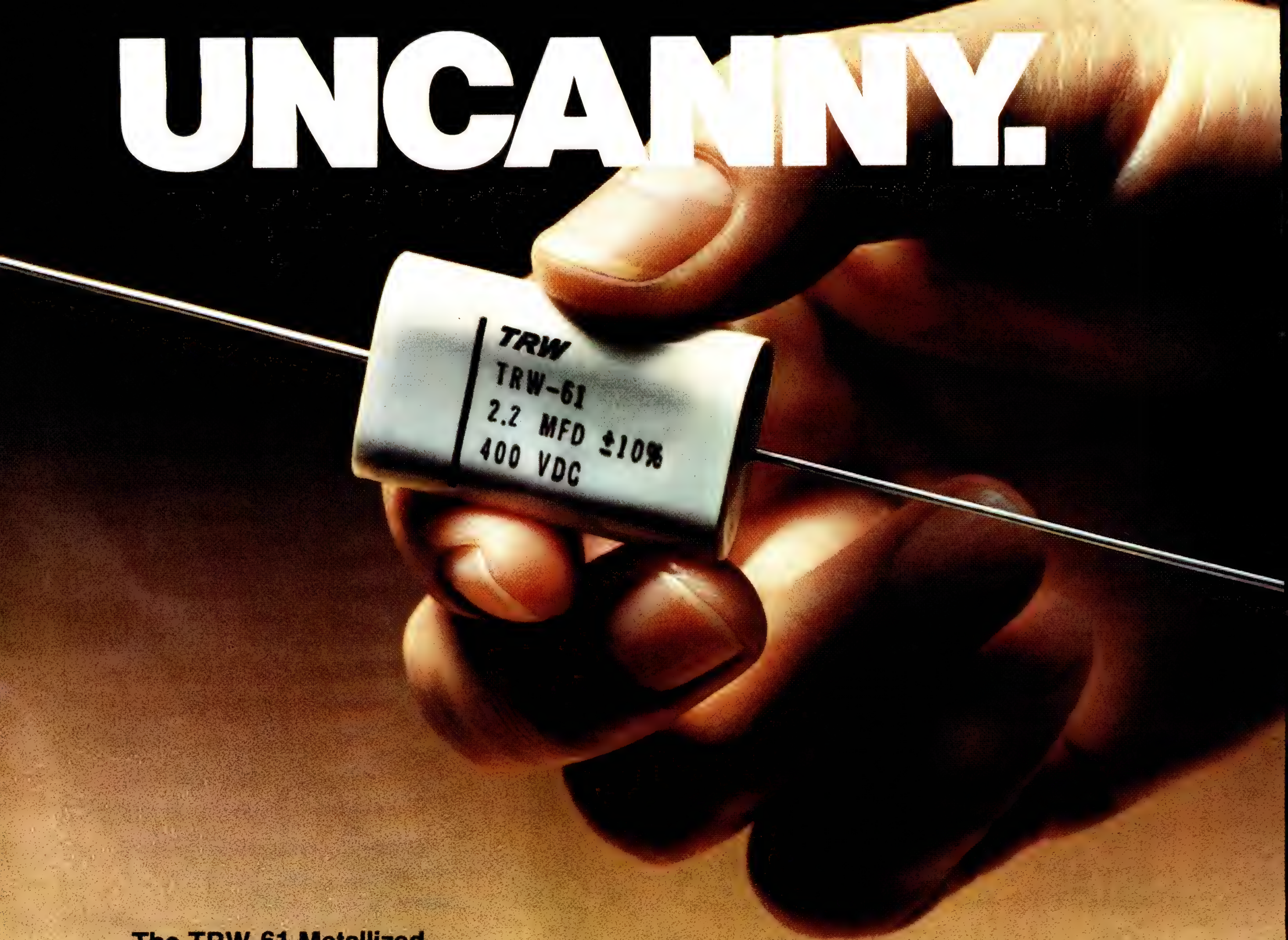

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Circle 98 on reader service card

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Bay State firms ponder their future

Business is booming right now around Route 128, but executives at electronics firms nonetheless have qualms about taxes and export controls

by Karen Berney, Washington bureau

All along Route 128, the high-tech road that rings the western suburbs of Boston, the economic recovery is in full swing and business is booming.

The exuberance that goes with good times will undoubtedly set the mood at Electro/84, slated for mid-May this year at Boston's Bayside Exposition Center and the Hynes Auditorium (see "It's Electro time again in Boston," p. 100). Executives from Bay State electronics firms making the rounds of the show will surely catch the glow.

Back in the privacy of their offices, optimism about the economy gives way to worry about the changing political milieu for doing business in the Commonwealth. So intense are these concerns—mostly about local political action—that many executives are taking time from their busy schedules to address these issues, so that this year's economic rebound—and the promise it holds for 1985—does not fade away.

Bluntly stated, "There is nothing good about the business climate for high-tech industries in Massachusetts," according to Edson D. DeCastro, president of Data General Corp., Westborough.

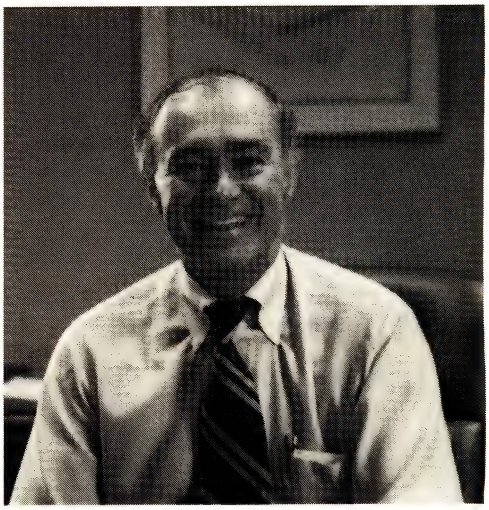
What alarms DeCastro and many of his colleagues at Route 128 firms are several local initiatives that, if cleared by the state legislature, could result in higher corporate taxes, as well as the state's further penetration into the affairs of private industry. These proposals spring from the administration of Governor Michael Dukakis, who has been feuding with the Route 128 community ever since returning to office a year ago.

Nor is Route 128 any more enamored with Washington. Topping the community's complaint list are new export licensing procedures proposed by the Reagan administration to clamp down on illegal technology transfers to Soviet-bloc countries. Massachusetts executives do not doubt the need to maintain the country's national security. However, they say, imposing tighter controls on an industry that typically chalks up from 20% to 40% of its revenues overseas would actually hurt this country and benefit others.

Signals. For now, however, and at least until after the November elections, neither state nor national politics is expected to dim business prospects. And despite the Route 128 community's irritation on a number of local issues, the electronics industry shows no signs of leaving the Bay State. On the contrary, this decade has seen the high-tech industry expand and hire new workers in Massachusetts at a fast clip. How long will the boom last? That depends first on the economy as a whole and, second, on the kind of signals sent out by Governor Dukakis, company executives claim.

By all accounts, it appears that 1984 will be a very good year for Route 128-area companies, particularly the computer manufacturers. Nationwide, this year's sales of computer systems will approach $44.5 billion, a 14% gain over 1983's $39 billion, predicts Creative Strategies Inc., a market research firm in San Jose, Calif. Growth in the New England region will outstrip the national average by seven percentage points and top $4 billion, just $1 billion less that what has been forecast for California's system vendors, Creative Strategies says. "Going gangbusters" is how observers often describe the current bonanza in this region's high-tech heartland. Evidence that renewed growth is well under way is now being confirmed by 1984's first-quarter results (see chart).

Among computer makers, Wang Laboratories Inc., in Lowell, reports that sales increased by 38% over the same period last year, to $543.5 million, and that new orders are up by 35% over last year's. Data General's profits more than doubled, to $12.6 million, and revenues grew by 33%, to $248.4 million, as the company


"There is nothing good about the business climate for high-tech industries in Massachusetts," claims Data General president Edson D. DeCastro, who is worried about governmental interference.

managed a performance comeback. DeCastro says yearly revenues will grow by 20% to 25% through the end of the decade. Apollo Computer Inc., in Chelmsford, whose sales soared from $18.1 million in 1982 to $80 million in 1983, is making no forecasts but describes financial analysts' estimates that revenues will double this year and grow by 55% in 1985 as "conservative."

Teradyne Inc., Boston, sees first-quarter sales jumping by 50%, to $80 million, to sustain an overall annual growth rate of 40% for 1984. M/A-COM, Burlington, reports first-quarter sales of $168.5 million. While this is only an 11% gain over last year's levels, the firm piled up a $179 million backlog. In addition, M/A-COM sees sales of digital communications, its fastest-growing product area, increasing at a 40% annual clip.

Route 128's defense contractors, who generated $6 billion worth of business for the state last year, see their sales growing in the 15%-to-20% range. The growing electronics content of new weapons systems is driving much of that growth, since the military cannot afford to be without the improvements in cost, efficiency, and reliability that come with electronic smartness, says William Farnsworth, vice president of government operations for Raytheon Co., in Lexington.

Increased spending by U. S. corporations on capital goods has been the key to better times—especially for many Route 128 manufacturers, since they build the components and systems industries need to stay productive and competitive. So unless a sharp rise in interest rates chokes off capital spending, demand for high tech should remain strong well into 1985, reports Julie Nickerson, a vice president with the Bank of Boston.

Keeping pace. In an effort to keep pace with accelerated technological change, New England high-tech companies will pour 32% more money than they did last year into expanded manufacturing and plant equipment, according to bank figures. The bulk of this money will go into defense-related businesses. In Massachusetts, defense contractors will increase spending by 57%, to $689 million from $439 million. M/A-COM, for example, has just opened a $25 million, 170,000-square-foot gallium arsenide semiconductor facility in Lowell. Last month, Raytheon began construction of an 80,000-ft^2 research and development and production center for very high-speed integrated circuits. Microwave-component-device manufacturer Alpha Industries, Woburn, is putting an 85,000-ft^2 production and engineering facility in Methyn. By December, GTE Strategic Systems division plans to relocate 200 engineers from its *headquarters* in Westborough to a new 60,000-ft^2 facility in Billerica, to work on a six-year $1 billion project to upgrade the Pentagon's worldwide command-and-control information system.

By contrast, capital investment by the Bay State's nondefense high-tech companies will drop by 1.4%, to $70.5 million from $71.5 million, says Nickerson. Part of that decline is accounted for by the heavy outlays made by industry in Massachusetts during 1981–82, she points out. But it also underscores the fact that companies are investing in other New England states. "Firms which favored Massachusetts as the site of their start-ups are expanding in adjacent areas, where the labor crunch is not as severe," she surmises.

As with other high-tech areas of the U. S., labor is of paramount concern to Massachusetts companies. As prosperity returns to Route 128, companies are stepping up their hunt for the engineering talent needed to keep the momentum going. With integration and compatibility now the computer industry's buzzwords, it comes as no surprise that experienced software programmers, especially those familiar with AT&T Bell Laboratories' Unix operating system, are at a premium. According to a survey conducted by the Boston Globe, entry-level software engineers are drawing the industry's highest salaries, at $29,000 a year; those with four years of experience command $40,000. At $28,800, data-communications programmers rank second in starting salaries.

"Software that is easy to service and use is becoming more and more important to the success of traditional hardware vendors," says John Adams, a computer analyst with Boston's Adams, Harkness & Hill Inc.

Route 128's demand for software talent is spiraling, and efforts to attract the qualified warm bodies span a broad spectrum. This year GTE Strategic Systems hopes to hire 400 engineers with backgrounds in local networks and systems integration. Recruitment methods range from paying bounties to employees who bring new people into the company to sending potential candidates infor-

It's Electro time again in Boston

The U. S. electronics community will congregate in Boston this month as the city hosts Electro/84, the annual East Coast trade show for electronics and computer products. An estimated 50,000 visitors are expected to attend this year's conference, which will be held May 15–17 at the Bayside Exposition Center and Hynes Auditorium. About 1,300 exhibits will feature such products as active and passive components, production and packaging equipment, instrumentation and test equipment, and fiber-optics systems. In addition, the Mini/Micro Northeast conference, held in conjunction with Electro, will feature exhibits on computer hardware and peripheral subassemblies, data communications, and computer graphics. A special marketing conference on the evolution and future outlook of electronic distribution will be held on May 15. An export marketing symposium designed to help electronics firms boost their business abroad will be held on May 16. The keynote speaker on May 15 will be Dr. John P. McTague, deputy director of the Office of Science and Technology Policy, in the Executive Office of the President. Dr. McTague will discuss "Nurturing the talent for U. S. competitiveness."

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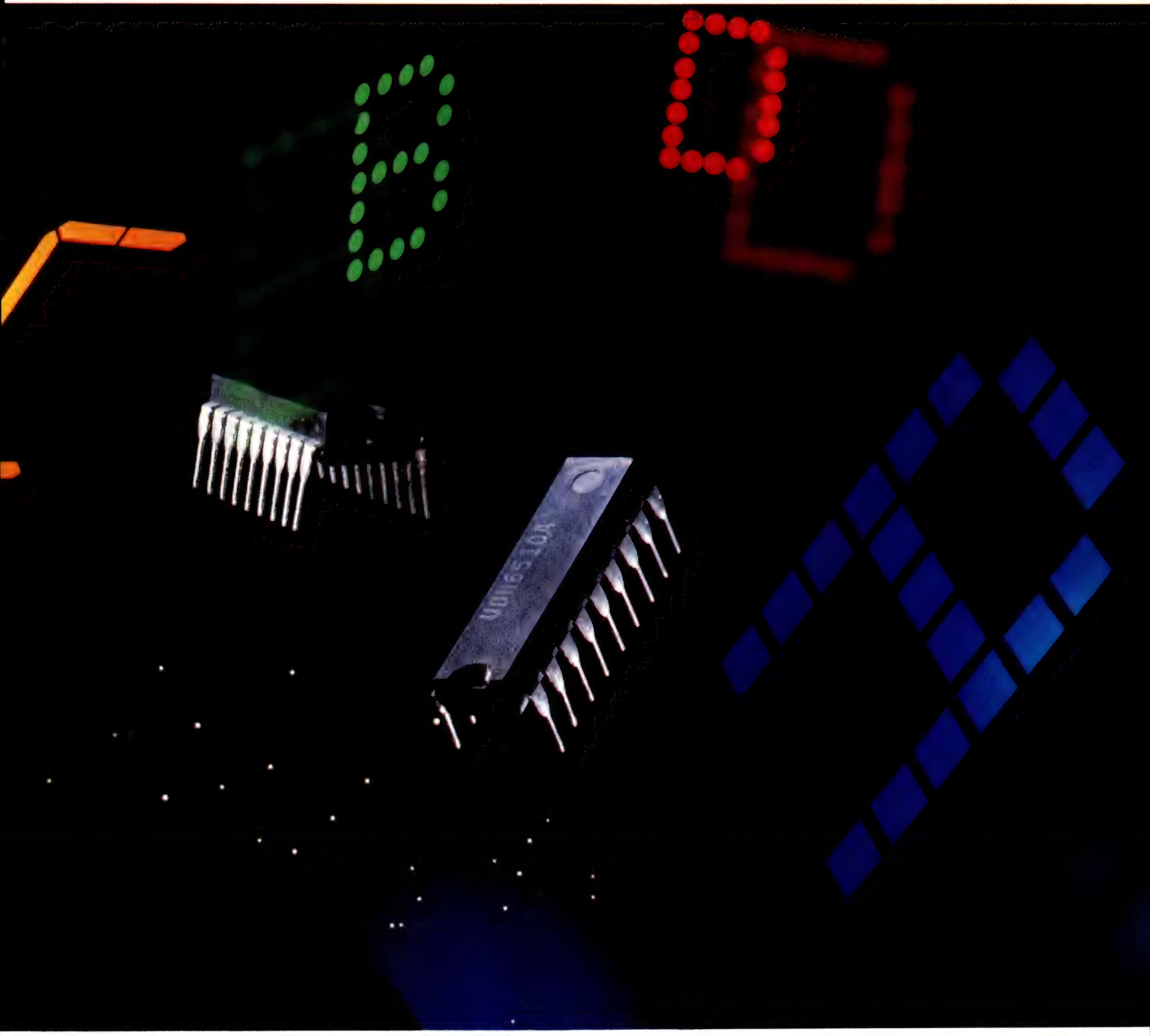

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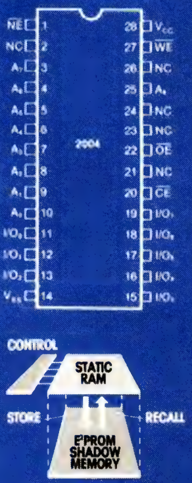

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mation packages containing color photographs of New England's fall foliage. Despite these efforts—to say nothing of open houses, advertising campaigns, and headhunters—GTE reports that as of mid-April, *it had* met only 22% of its new-hiring goal.

The exploding demand for software engineers is bad news for Andrew A. Kariotis, president of Alpha Industries. Kariotis claims that in response to engineering shortages in the computer field, universities have established or expanded computer science departments at the expense of traditional engineering endeavors. Consequently, "there is a dearth of microwave-circuit engineers," and as a result, companies that need them have "simply bid their salaries out of sight," he claims. The survival of the U. S. microwave industry, "unfortunately, may depend on licensing technology from Japan," to which the U. S. has conceded leadership, he says. Despite the impact that manpower shortages could have on growth, Route 128 is confident that 1984–85 will be a peak year for sales and earnings.

Politics. While the good times are here, however, Route 128 executives share the view that the greatest uncertainty they face concerns the direction the state government will take in its dealings with private industry. "What are at stake are decisions on a number of issues that will affect Massachusetts' future as a mecca for high-tech industries," claims Howard Foley, president of the 150-member Massachusetts High Tech Council (MHTC).

Most inimical to high-tech development, he asserts, are the governor's tax policies. At first it was Governor Dukakis' intention to step up enforcement of unitary taxation—assessment of corporate income taxes on a worldwide versus statewide basis—that was raising the industry's ire. That proposal was recently abandoned in favor of a package touted by the governor as a "compromise solution." In exchange for repealing the unitary statute, industry was recently asked to support the establishment of the Massachusetts Development Bank (known as MassBank), meant to undertake badly needed repairs in the state's infrastructure. Funding to the tune of $145 million by 1995 would be raised by increasing the corporate excise tax to 10%, from 9.5%, and the tangible property tax to 3.6% per $1,000 worth of property, from 2.7%. In exchange, unitary taxation has been traded off for a new version that will tax businesses on their total domestic U. S. (versus worldwide) earnings.

"We have no taste for writing a check for projects that should be financed by the public at large . . . nor do we think the state has any right to tax the profits on our operations outside of the Commonwealth," argues Kariotis, in a statement that sums up the sentiments of all. Thus, in a move that stunned the state house, the 14-member executive board of the MHTC took an early April vote that rang a unanimous "no" for the MassBank.

SELECTED ROUTE 128 COMPANY REVENUE GROWTH

Company	1983 Total revenues	1984 1st quarter revenues	1984 1st quarter growth (%)	1984 Growth estimate (%)
	(millions of dollars)			
Alpha Industries Inc.	52.2	17.0	23	25
Apollo Computer Inc.	18.1	36.6	225	125
Data General Corp.	829.0	248.4	33	27
Digital Equipment Corp.	4,270.0	2,000.0	38	30
M/A-COM Inc.	654.3	168.5	11.2	20–30
Prime Computer Inc.	516.5	145.0	21	25
Raytheon Co.	5,930.0	1,570.0	14.5	20–25
Wang Laboratories Inc.	1,530.0	543.5	38	38

SOURCES: COMPANY INFORMATION; 1984 GROWTH RATE ESTIMATES FROM DEAN WITTER REYNOLDS INC.

Executives do not believe that the MassBank or the increased corporate taxes to fund it will themselves cause an exodus from the state by high-tech firms. The real threat is that higher taxation could become "the factor that tips location and expansion decisions away from Massachusetts," Foley believes.

An indication of what could happen if the tax situation sours comes from Florida. One year ago, Florida started collecting unitary taxes. International Business Machines Corp. and Pfizer Inc., both of which had expanded into the state before the imposition of unitary taxation, canceled plans to expand their operations further. Now Florida is looking at a law to eliminate unitary taxation altogether, Foley reports. At least half a dozen high-tech companies—among them IBM, Augat Inc., Sony Corp. of America, and Teradyne—have said they will not start up new facilities in Massachusetts until they see how the vote goes on the MassBank.

Another proposal that irks Route 128 companies is mandatory notification to the state of any plan for plant closings, layoffs, or relocation. Foley contends that such legislation is not only presumptuous—since it assumes that a bureaucrat can salvage what a businessman could not—but would also place Massachusetts at a disadvantage to states that do not have such laws. In addition, prenotifying the state would tip off the competition about business moves. After nine months of intense negotiations, the state is coming around on a compromise proposal under which management and labor would voluntarily agree to work together to minimize the disruptions associated with layoffs or plant closings.

Leave us alone. "The bottom line is that the primary mission of high-tech companies is to run their operations. Instead, they find themselves devoting an increasing number of man-hours to convincing state economic planners that their legislation is bad. That accomplished, they then have to put in overtime to hammer out alternative legislation that ensures representation of their interests," argues Charles Baker, director of communications for the MHTC.

Even the few state initiatives that could be construed as favorable to high-tech elicit few cheers from the industry. The industry's battle with Washington over export licensing is

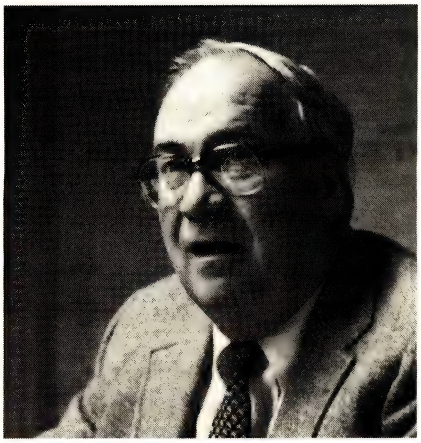
one example. Prime Computer Inc., Natick, is looking to earn 50% of its revenues abroad this year—a 20% increase over 1983. Washington's imminent clamp-down on exports could mean disaster for Prime and other high-tech firms. Enactment of regulations that would require case-by-case review of every product shipped overseas would not only cause existing customers to go elsewhere but also discourage new customers from buying in the U. S., believes Prime's vice president of corporate business development and strategy, Gale Aguilar.

On this issue, the state and high-tech companies appear to be in synch. Governor Dukakis, claiming that the proposed licensing changes would cost the state 20,000 high-tech jobs and $2 billion in revenues in one year alone, has diligently fired off protest letters to President Reagan. But as far as those on Route 128 are concerned, their cause would be better served if the Democratic governor would simply take it easy. "Due to his less-than-amiable relationship with the President, private industry feels that it would be best helped if he was working behind the scenes," suggests an industry spokesman who asked not to be named. "Instead, he has seized on the issue as a chance to publicly embarrass the Republicans."

The state's plan to put up half the funds for a $40 million microelectronics center is another target for Route 128 antigovernment crusaders (see "Massachusetts antes up for chips"). Potential sites for the center have been narrowed down to Marlborough, Westborough, and Taunton. The first two are located at the crossroads of interstates 495 and 290, in the heart of the Route 128 area, and they are central to the computer companies that will be contributing teaching engineers and equipment to the facility. Taunton is in southeastern Massachusetts and the furthest away from Route 128. But because Taunton is experiencing substantially higher unemployment than the state's 5% average and is economically depressed, Dukakis is pressuring the site-selection committee to choose it, industry reports. Should Taunton win, Data General's DeCastro says he will be the first among many to withdraw corporate support from the center. It is straight politics, laments MTHC's Baker. "The governor has no inclination to let the issue come to a vote until he has the [necessary] votes," he says.

"With these issues before us, it will be difficult for any industrial firm to explore further expansion in Massachusetts or locate here for the first time," warns DeCastro. However, some of his natural allies think he may be overstating the case. Massachusetts' reputation for academic excellence and a high quality of life will continue to lure investment in spite of the business climate, goes the more moderate position.

Still another angle comes from an executive at Teradyne, who argues that Route 128, like California's Silicon Valley, is becoming a victim of its own success. The lesson to be learned is that when a segment of industry concentrates in one particular area and refuses to spread the wealth around, the costs of land, labor, and general living skyrocket. That is beginning to happen in the approximately 100 square miles that surround Route 128.



A dearth of engineers may force U. S. firms to license foreign technology, thinks Alpha Industries president Andrew Kariotis.

Massachusetts antes up for chips

While the Route 128 business community and the administration of Governor Michael Dukakis may wrangle over politics, they do share one overriding economic goal: keeping the state's high-tech juices flowing.

That goal may be realized in the Massachusetts Microelectronics Center (MMC), to be set up with matching contributions of $20 million from state and industry. Through the center, industry will claim a stake in the high-technology future, and the state government will get a catalyst for new jobs and economic growth.

According to Joseph Stach, the center's newly appointed director, MMC is an attempt to address that aspect of technology most neglected and needed by the Route 128 community: semiconductor design and processing knowhow. "With the trend toward integrating computer functions on a single chip, semiconductor development is becoming an increasingly important component in computer-system manufacturing. The state has to be prepared to serve that need or else risks losing in the nationwide competition for high-tech investment," he explains.

The center is not intended to produce technological breakthroughs, though it will focus on next-generation devices, such as a 4-megabit chip, notes Stach. Its charter is to offer engineering students at nine participating universities a hands-on up-to-date experience in computer-aided design, as well as the commercial processing and fabrication of integrated circuits. Courses should begin in the 1984–85 semester and will be offered through a computer link-up to the nine universities. A total of 1,500 students could be enrolled, and an instructional processing lab will be operational sometime in 1986.

Stach expects that MMC will eventually foster the development of a local semiconductor industry; but the most immediate benefits will accrue to the Route 128 community. The supplemental training will make it easier to put graduates straight to work by minimizing on-the-job instruction and learning, he stresses. **—Karen Berney.**

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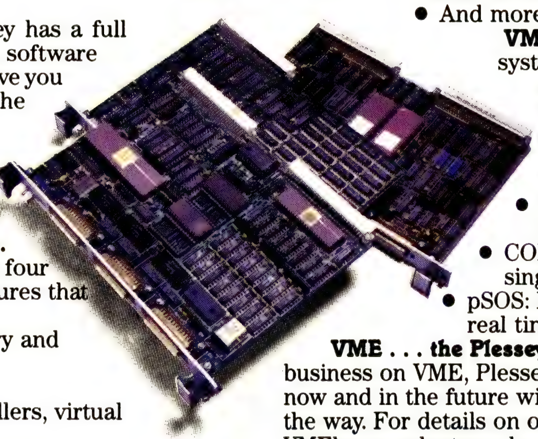

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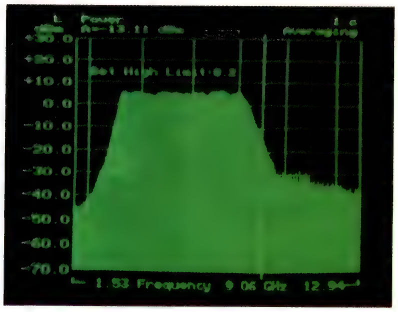

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Telecommunications

Italians chart path to ISDN

The hardware for integrated-services digital networks has begun to emerge, but it will be several years before the economics permit massive introduction

by Robert T. Gallagher, Paris bureau

The hordes of tourists who flock to Florence every year come mostly to savor the city's awesome array of Renaissance buildings and fine-arts treasures. But the 1,800 or so telecommunications engineers from all over the world who will converge May 7–9 at the Palazzo dei Congressi, near the famous Uffizi Gallery, will have a different kind of architecture on their minds: the architecture of integrated-services digital networks (ISDNs). They are heading to Italy for the 11th International Switching Symposium (ISS), sponsored this year by the Italian ministry of Posts and Telecommunications.

Few people in telecommunications would deny that ISDN's impact on the business will be rivaled only by that of the telephone itself. At this year's ISS, much of the technical program will be devoted to elocutions by executives of the companies that make telecommunications-switching equipment, who will explain why their particular digital switch is best suited to take part in the industry's march to ISDN. Several companies will be showing off experimental ISDN configurations.

What services? There is still some disagreement about just what services ISDN should provide. It is certain that with digital networks in place, telephone companies will be able to offer subscribers such services as data access and transmission, facsimile, and even video-telephones and -conferencing. These services will be introduced gradually, with data and facsimile becoming available in a number of countries as early as 1986. In addition, the quality of standard telephone service will rise steeply.

Not surprisingly, the country making the most noise about its plans for a network is the host, Italy, both for logistical and political reasons.

Although all the companies scrambling for market shares in European telecom markets [*Electronics*, Oct. 20, 1983, p. 106] will be on hand at Florence, the most impressive live ISDN demonstrations tied to the ISS will be presented by two Italian outfits: Italtel Società Italiana Telecomunicazioni SpA and Face Standard SpA, ITT's Italian telecommunications subsidiary. Both demonstrations will be based on installed switches.

ICs wanted. Italtel's R&D chief, Maurizio Dècina, says VLSI chips for protocols and echo canceling are crucial to integrated digital networks.

"We're not talking about experiments and feasibility studies here; we're talking about business," asserts Maurizio Dècina, Italtel's director of research and development.

While Dècina admits that the proliferation of ISDN experiments might lead people to believe that such services are just around the corner, he notes that ISDN is not likely to be economically (as opposed to technically) feasible for at least another two years. "Before anyone can make money offering ISDN services, he has to have access to three key VLSI circuits," he explains. (See "The long climb from twisted pairs to wideband services," p. 108).

Dècina says that in an ISDN environment such as the one currently being defined by the International Telegraph and Telephone Consultative Committee (CCITT), in Geneva, subscriber units at local offices would be connected to a network termination by way of a two-wire loop operating at 144 kilobits a second. Using a passive bus, about eight subscribers would in turn hook into the termination.

"There are two essential protocol chips: one each for the subscriber terminal—the level-one D-channel protocol—and the subscriber module of the local office—the level-two protocol," says Dècina. "Then there is an echo-canceling chip necessary for either end of the two-wire loop." It is the echo-canceling chip, a kind of one-chip modem, that poses the most serious stumbling block.

Before integrated-circuit manufacturers take a shot at making money on these three complex chips, they want to see *international* standards that would justify the investment required by the ICs. Dècina, the chairman of the CCITT committee defining the IC standards, says that its work on the protocol chips is now complete but that much remains to be done on the echo canceler, which is easily the most complex of the three.

When CCITT transmission standards were set at 144 kilobits per second—two principal channels of 64-kb/s and a third, 16-kb/s channel for signaling information and some data transmission—echo canceling became indispensable. The only conceivable alternative, a ping-pong arrangement, where data is transmitted in bursts in alternate directions, is out of the question at that transmission rate.

At ITT Europe Inc., in Brussels, Renaat Van Malderen, marketing manager for the company's system 12 digital switch, agrees with Dècina, explaining that ITT has integrated some of the protocols onto three large-scale ICs. "But what you really need to be able to offer ISDN economically is VLSI," he admits.

Other snags. Van Malderen sees other snags that must be ironed out before ISDN can be offered widely. "In addition to an inexpensive digital subscriber loop that works, there's a need to develop a lot of additional software to make ISDN compatible with a normal telephone exchange," he notes.

"And, then, we don't really know what effect the increased call rate caused by ISDN is going to have on the network, so there is going to have to be a very powerful control mechanism, and of course there is also the problem of mixing circuit switching and packet switching," Van Malderen explains.

Nonetheless, manufacturers of telecom equipment are quite sanguine that the problems can be ironed out during the next couple of years. Visitors to Florence will get a peek at the fruits of those labors when both Italtel and ITT vie for visitors to their ISDN demonstrations, scheduled for Florence and Bologna, respectively, on Wednesday, May 9.

Ping pong. Italtel will be demonstrating bidirectional transmission on a digital line with one 64-kb/s channel plus a 16-kb/s signaling channel, a setup that was favored to be the ISDN standard several years ago. Without the second 64-kb/s channel, the company will be able to transmit with a ping-pong arrangement using burst-mode line modems suited to existing subscriber loops of up to 3.5 kilometers.

The switch Italtel uses is its UT10/3 exchange [*Electronics,* April 21, 1981, p. 86]. For the experiment, Italtel added to the exchange a packet-handling module that performs data-subscriber interconnections, data-trunk interconnections, B- (circuit-switched) and D-channel (packet-switched) handling, packet routing, operation, and maintenance. Two Z80 microprocessor-based microcomputers (a front-end system and another one), common to all lines, ensure digital line interface.

Other circuit-switched services that Italtel will be showing include pulse-code-modulation telephony with a signaling protocol that permits the identification of the calling subscriber and a variety of diagnostics; data transmission, such as teletex; and multiservice terminals for mixed-voice and nonvoice communications. Packet-switched services will include such configurations as X.25 terminals connected to the B-channel and packetized data terminals supported on the D-channel. This makes it possible to have videotex and alphanumeric terminals interfaced at the subscriber's premises to a protocol adapter that provides D-channel access.

Face to Face. ITT's demonstration will be similar, though the company will be transmitting at 144 kb/s with an experimental 1240 digital switch installed by Face Standard. It will operate facsimile, teletex, and PCM telephone services in an environment that, like Italtel's, includes standard analog telephone service.

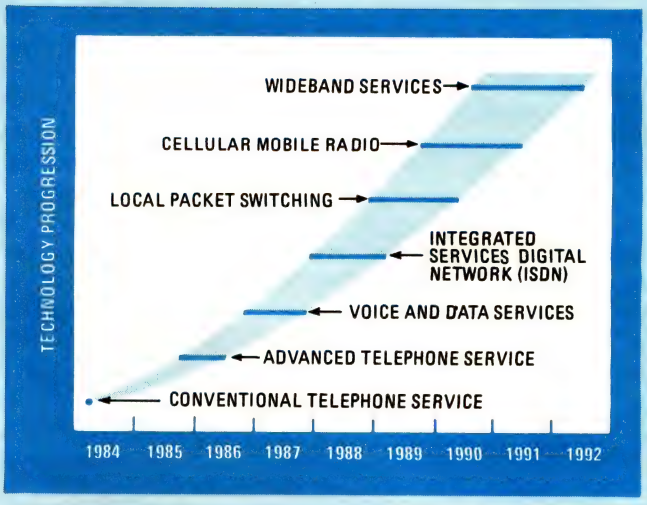
Above all, ITT will try to make the point that its system 12, with distributed architecture, is better suited to the country's evolution to ISDN than systems controlled by an external computer. In the case of Italtel, ITT may well be preaching to the converted, as the Italian company's presentation of its competitive UT/100 will boast about the advantages of its modularity. ☐

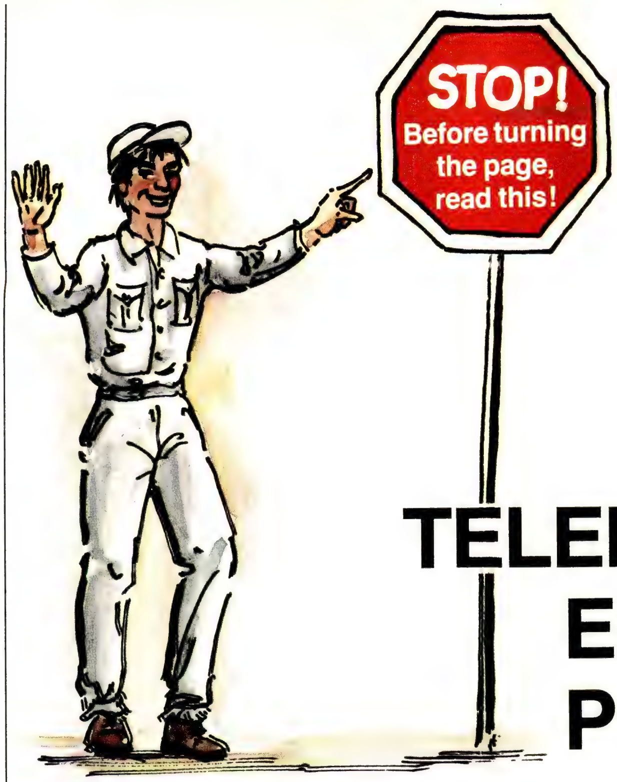
The long climb from twisted pairs to wideband services

Italtel, Italy's state-controlled supplier of telecommunications equipment, has developed a long-term proposal intended to push the country's telecommunications infrastructure to state-of-the-art levels of technology. Right now, that infrastructure is the least advanced among the major countries of Western Europe.

The company wants to upgrade today's ordinary twisted-pair telephone services and make wideband digital services available by the 1990s. The plan calls for the Italian telephone-operating company SIP to start offering voice-band data circuits around mid-1986. The first phase of the integrated-services digital network would be put in place between late-1987 and mid-1989.

As the ISDN is built up, local packet switching will be introduced. Early in 1989, cellular mobile radio will take a bow. Wideband transmission services should become available in mid-1989.

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Information processing

Business takes to videotex

So far, there has been no groundswell by consumers for videotex, but business use of interactive computer-video services is catching on fast

by Wesley R. Iversen, Chicago bureau manager

Although videotex has long been ballyhooed as a lucrative consumer market that is just around the corner, the technology may well find a home in the office more quickly than it finds one in the living room.

The trend was evident at mid-April's Videotex 84 show in Chicago, where major vendors—including Honeywell, DEC, and AT&T—rolled out products aimed specifically at business-videotex applications. "Videotex will arrive in the home eventually," predicts David Cleary, vice president of small-computer marketing for Honeywell Inc. in Boston. For the short run, he feels that "the Fortune 500 type of user is the easiest to identify in terms of the payoff."

To be sure, there are still plenty of dollars chasing after the consumer market and promising a plethora of services, from home banking and shopping to electronic newspapers and other forms of information. Joining the first commercial system, rolled out by Knight-Ridder Newspapers in Florida last fall, consumer-oriented videotex systems based on the graphics-rich North American Presentation Level Protocol Syntax (NAPLPS) are set for launch this year in Chicago and Southern California. Moreover, recently announced plans by corporate heavyweights IBM, CBS, and Sears, to uncork a nationwide consumer-videotex service later in the decade give additional impetus to the home-videotex idea.

Yet the home videotex market will probably require a few years to develop momentum, while many at the Chicago show agreed a bustling market for business videotex is here today. Paul E. Vogelsang, associate director for videotex research at Arthur Andersen & Co., in Milwaukee, says his consulting and accounting firm has helped about a dozen large companies set up internal videotex systems since the trend began two years ago. In Schiller Park, Ill., Honeywell's videotex program manager, Raymond T. Oschger, anticipates a business-videotex market of "several hundred million dollars annually" for perhaps the next 10 years.

That may look like small potatoes next to the multibillion-dollar markets projected for consumer videotex. But it was big enough to prompt Honeywell to set up a videotex support center in Schiller Park six months ago and to introduce two business-videotex systems at the Chicago show. About half a dozen businesses are working at the center and experimenting with their own videotex data bases. Mainframes and support services are provided by Honeywell.

"The rationale for business videotex is that we [the computer industry] have made standard retrieval systems too damn hard to use," explains Oschger. Because of its menu-driven format, videotex can be accessed easily, even by intermittent and unsophisticated users.

Corporate communications. The technology is a prime candidate for helping to keep employees outside of data-processing departments—including far-flung sales staffs—informed of product and pricing announcements, corporate policy changes, and the like. Salespeople can also enter orders using the videotex two-way capability. Fast, cost-effective systems can also be set up to communicate with customers, suppliers, and agents, proponents point out. When tied into existing corporate data bases, videotex systems can help managers make decisions by providing quick access to the latest financial information.

Externally generated information seems to be important for internal

Information, please. CompuServe Inc. operates a private videotex service that can link businesses to their customers and prospects through a data base in Columbus, Ohio.

business systems as well, says William W. Seelinger, manager of videotex market development at International Business Machines Corp., Armonk, N. Y. Like Honeywell, DEC, and other firms pursuing the business-videotex market, IBM is experimenting with its own internal videotex system. At IBM, the top three services, viewed by some 400 users on the system, are the Dow Jones News/Retrieval Service, the Official Airline Guide, and IBM Bulletin Boards, says Seelinger, who is also a board member and chairman of the United States Videotex Industry Association. During meetings at the Chicago show, the association set up a separate Business Videotex Council, another indication of growing interest in the business-videotex field.

Linking groups. Videotex technology has also been opening opportunities for third-party systems operators who want to capitalize on the business market by linking "closed user" groups, such as customers and suppliers. CompuServe Inc., a Columbus, Ohio, supplier of ASCII-based on-line data-base services, has such a private videotex service that includes NAPLPS graphics. Another example is the Videolog service, from Videotex Information Corp., Wilton, Conn. [*Electronics,* Sept. 8, 1983, p. 51]. A NAPLPS-based catalog service that allows electronics design engineers and purchasing agents to access product information that has been put into the system by electronics manufacturing firms, Videolog is set for commercial launch at this fall's Wescon, in Anaheim, Calif. At Videotex 84, Videolog was among packages used by Wang, IBM, and DEC to demonstrate the capabilities of new software offerings that let personal computers act as videotex terminals.

Also at the show, Wang Laboratories Inc., Lowell, Mass., made its videotex debut by introducing a $250 package called Viewdata Decoder, for use on the Wang Professional Computer. IBM showed its recently announced PC/Videotex software, priced at $250 for the Personal Computer and the PC XT, and $220 for the PCjr [*Electronics,* April 19, p. 67].

Digital Equipment Corp., of Maynard, Mass., used the show to introduce such products as two new videotex software packages for its Professional 350 desktop minicomputer. PRO/NAPLPS costs $195 and lets the 350 access outside videotex services. PRO/Videotex, billed as the first stand-alone videotex system available for a desktop computer, sells for $895. Developed by the Genesys Group Inc., Ottawa, Canada, PRO-/Videotex lets a data base of about 5,000 videotex frames be stored on a 10-megabyte Winchester disk for resident access, thus eliminating communications charges encountered with conventional videotex systems that require on-line connection to a remote host. Data on the disk can be updated either by flexible disk or from a remote host, at night, when communications costs are low.

Host of images. Such stand-alone hardware as DEC's PRO/Videotex stores pages of graphics information locally on disk, or calls them up from remote mainframes.

DEC also introduced a business-videotex software system called VAX VTX, which runs on VAX machines under the VMS operating system and can be used with the company's ALL-IN-1 office-automation system. The full package will be available in June for a $25,000 licensing fee.

Dedicated Sceptre. As for AT&T Information Systems, it stuck by its dedicated Sceptre NAPLPS-compatible videotex terminal, part of the AT&T Videotex Information System introduced at the show. This is a turnkey package of components designed to help business users and other institutions create private videotex systems. To be available in September for $140,000, the package includes 10 Sceptre terminals, as well as a frame-creation system, a minicomputer for data storage, an administrative terminal, and an ASCII printer for control and programming functions.

Sam Berkman, AT&T division manager for consumer sales and service, in Parsippany, N. J., emphasizes that the firm's videotex focus remains "clearly on the consumer business." He does concede that interest at the show in the new business system was higher than expected. The inquiry rate suggests that "if we have any kind of problem, it's going to be in delivering," Berkman notes.

Tougher competition. Moreover, activity at the show suggests that competition in videotex terminals could get tougher before long. Chip makers Texas Instruments, Motorola, and Rockwell are among the firms working on NAPLPS chips that could drive down the cost of terminals. Panasonic was promising January deliveries on a terminal priced at less than $500.

Not everyone, however, believes that the jazzy NAPLPS-style graphics used in the consumer marketplace will be necessary for most business applications, since existing corporate data bases contain mostly textual material. Two business-videotex software packages that Honeywell introduced at the show reflect that kind of thinking: both of them feature European-style alphamosaic protocols, which produce cruder graphics than the alphageometric NAPLPS, but offer faster frame-transmission times.

A product called InfoNow, based on the French Antiope standard, was developed by a French firm, Groupe Française d'Informatique. InfoNow is designed to run as a dedicated business-videotex system on Honeywell DPS 6 computers. The other package, known as RETRVE, is based on the British Prestel standard and uses software developed by Thorn EMI, Feltham, Middlesex, England. This package was designed to coexist with other applications on Honeywell's larger DPS 8 system. Both packages will be available around midyear for a one-time licensing fee of about $30,000 to $60,000. □

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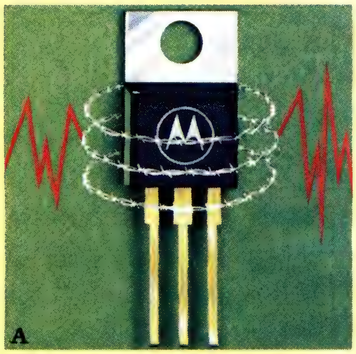

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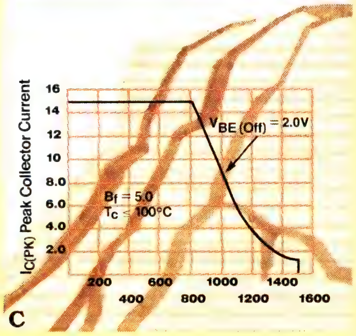

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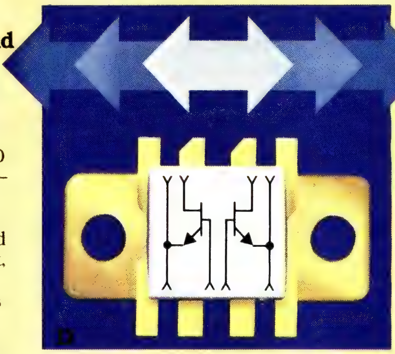

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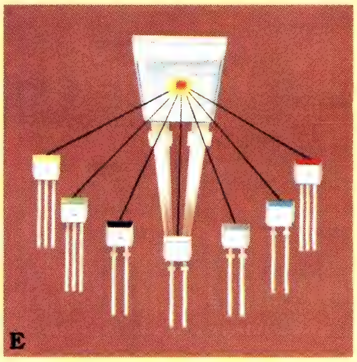

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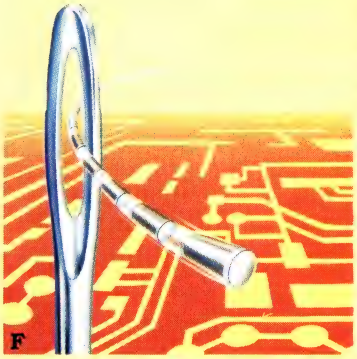

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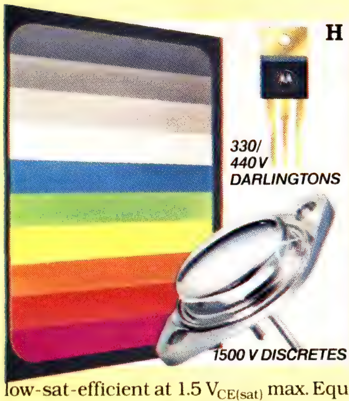

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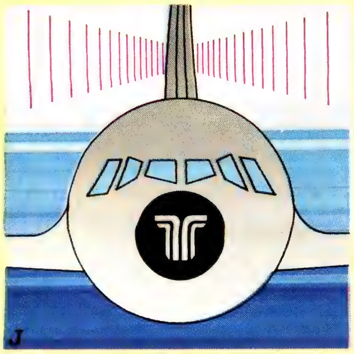

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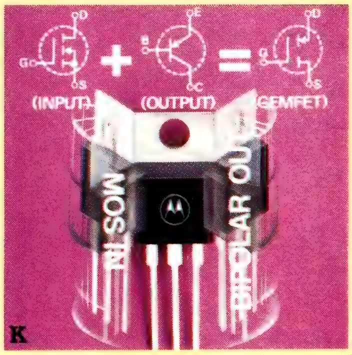

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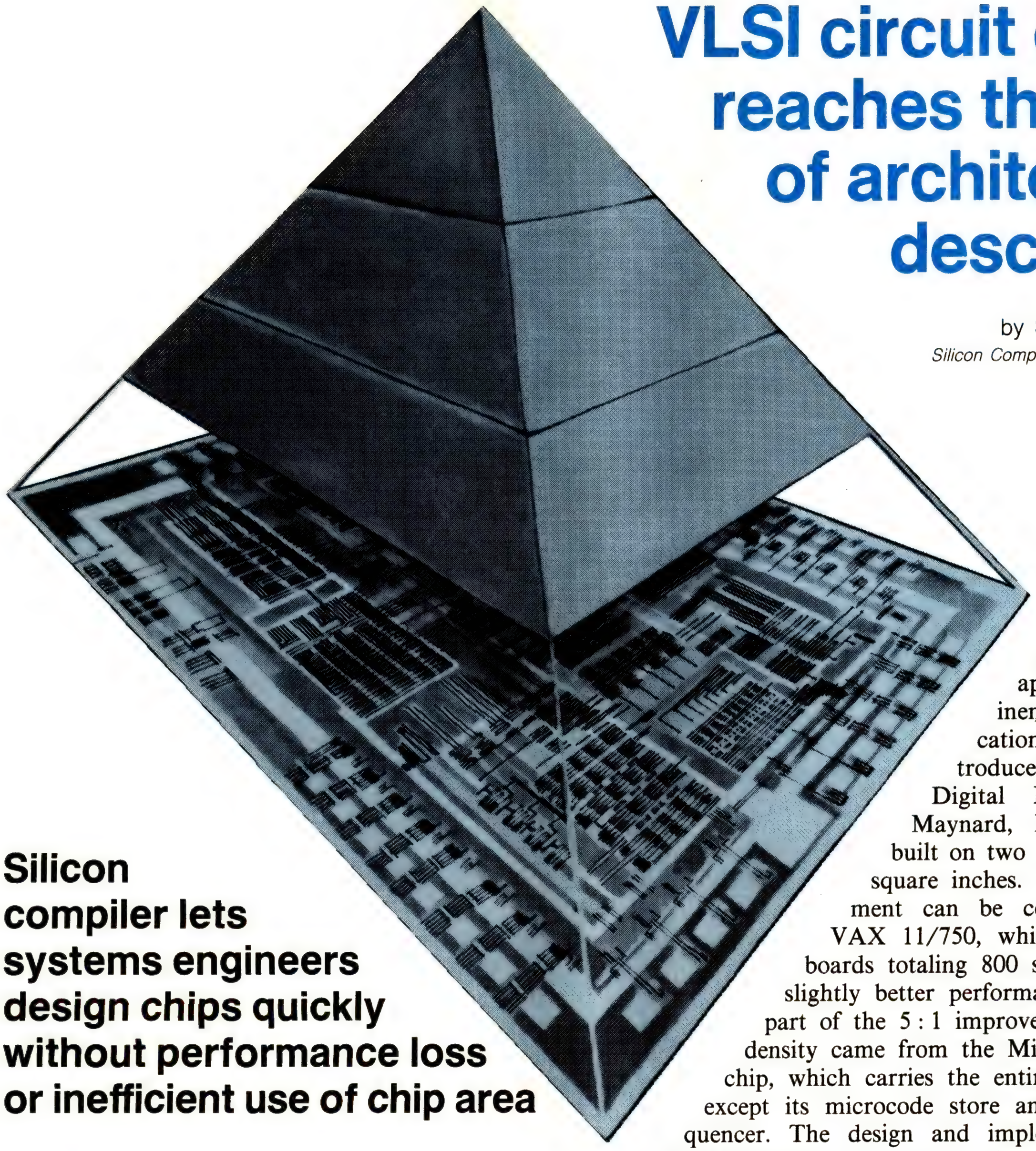
VLSI circuit design reaches the level of architectural description

by Stephen C. Johnson,
Silicon Compilers Inc., Los Gatos, Calif.



Silicon compiler lets systems engineers design chips quickly without performance loss or inefficient use of chip area

Silicon compilation, the process of automatically synthesizing complex designs and their analysis and verification models from high-level architectural descriptions of systems, is now capable of producing a wide variety of very large-scale integrated circuits that are of merchant-market quality. Virtually any systems designer can participate immediately in the design process. Furthermore, short design turnaround times and design simplicity do not occur at the expense of added silicon area.

Silicon compilation was first described in 1979 by David L. Johannsen (see "What is silicon compilation?" p. 122). Under the guidance of his thesis adviser, Carver Mead, at the California Institute of Technology at Pasadena, Calif., Johannsen demonstrated the practicality of silicon compilation for implementing certain types of VLSI architectures. Johannsen and Mead, along with Edmund K. Cheng, formerly of Intel Corp., Santa Clara, Calif., subsequently founded Silicon Compilers Inc. to further such research and explore the practical applications. One eminently practical application is the recently introduced MicroVAX from Digital Equipment Corp., Maynard, Mass., which was built on two boards totaling 158 square inches. This space requirement can be compared with the VAX 11/750, which consists of five boards totaling 800 sq in. and has just slightly better performance. A substantial part of the 5 : 1 improvement in functional density came from the MicroVAX's data-path chip, which carries the entire 32-bit processor, except its microcode store and control-store sequencer. The design and implementation of this 37,000-transistor IC took the three-member team and the proprietary silicon compiler only seven months. The n-channel MOS chip, which measures 98,000 sq mils, carries a 32-bit arithmetic and logic unit, a 64-bit barrel shifter, a control decoder, flag logic, a dual-port block of random-access memory housing 47 registers, a timer, a seven-level operand-restore stack, and a 32-word block of read-only memory (Fig. 1).

Until recently, silicon compilation continued to be viewed by many as simply an interesting research topic, with little promise of immediate practical value. The merchant-market IC industry, in particular, has shown little interest in new design methodologies, especially those that seemed to sacrifice silicon area or performance. This point of view is understandable in an industry that competes primarily on cost and performance. As a result, there has been little change in merchant-market IC design methodology in the last 15 years. Even computer-aided design, without which VLSI could not have come into existence, did not change the underlying design

What is silicon compilation?

Silicon compilation is a design-automation methodology that moves the process of realizing a merchant-market-quality very large-scale integrated circuit toward the architectural level and away from classical, microlevel considerations, so that systems engineers can effectively design chips. Silicon compilation encapsulates the knowledge of expert IC designers in the areas of layout, timing analysis, and functional simulation.

Just as software compilation synthesizes complex assembly-language programs from programs written in high-level languages, modern silicon compilation synthesizes critical views of an IC, such as layout (topology), functional description (simulation model), and performance (timing model) from high-level architectural descriptions. These descriptions are in terms of structures "known" to the compiler, such as programmable logic arrays, read-only and random-access memories, arithmetic and logic units, registers, or complete data paths. Structures can be described functionally (shall the ALU multiply?), in size (how wide is the data path?), or in terms of mathematical, logical, or state equations.

The structures themselves are actually synthesized from stored rules that are built into the compiler. The rules represent an attempt to embed the best of the IC designer's art and science, and when invoked by the compiler, yield a layout, a functional simulation model, a timing model for the structure, and ultimately, a timing model for the chip. Silicon compilation typically uses several thousand rules that will yield from 200 to 500 of the most useful high-level VLSI structures from about 40 different classes. Designs can be provided for different VLSI processes, and a specific compiler usually has a wide range of similar processes for which it can produce circuits with no user input other than process selection.

Architectures may be specified hierarchically, and the layout may be synthesized either hierarchically (wiring blocks into modules and modules into chips) or with the flat approach (working at the block level, wiring directly from one block to another). Interconnection routing is accomplished automatically by the compiler. Silicon compilation also uses an integrated hierarchical data base and provides complete functional simulation at any level of the design hierarchy automatically. It also produces complete performance reports and critical path analysis automatically from the completed layout.

During the design process, which is incremental by nature, silicon compilation provides estimates of a wide variety of circuit characteristics before they are fully determined. Finally, it puts out masking tapes and all supporting plots and documentation, thereby eliminating from the design process such steps as logic design, logic simulation, circuit design, circuit simulation, layout, postlayout parameter extraction and resimulation, electrical rule checks, and topological design-rule checks. Thus, *all* of the arcane aspects of VLSI design disappear, permitting a competent systems designer (in addition to a chip designer), to utilize silicon compilation to create merchant-market-quality custom or standard integrated systems.

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methodology. CAD simply speeded up, made more accurate, or changed the form of certain steps of a well-worn design path.

This lack of interest in silicon compilation by the IC industry is compensated for, however, by its potential for use by manufacturers of electronic end products—the systems houses (see "The application-specific IC market starts to grow," p. 124). These manufacturers look forward to the advent of a technology that provides rapid, accurate development by systems engineers of VLSI systems with no sacrifice of silicon or performance.

The MicroVAX project and two others—the development of a single-chip Ethernet data-link controller (EDLC), which is in commercial production by Seeq Technologies Inc., San Jose, Calif., and the RasterOp Controller used in the Sun II work-station products—have proven that such a technology is at hand.

Integrated systems technology

Silicon compilation sprang from efforts to develop an integrated systems technology that not only encapsulated the expertise and methodologies of the best designers in the IC industry, but provided higher levels of design leverage by means of radical new methodologies. The resulting technology bears little resemblance to layout-simplification methodologies now in vogue, such as standard cells or gate arrays. Instead, the technology addresses the entire VLSI design process simultaneously, and implements an approach practiced only in the more mature arts and sciences: design by successive refinement, or incremental design.

The term design leverage refers to processes or methodologies whereby small inputs of time or effort by a designer result in large amounts of high-quality, useful design output. For example, if a methodology will permit three designers to produce a working 37,000-transistor chip in six months, when classical methods require a combination of 20 engineers and layout draftsmen working for two years, that methodology has leverage.

Current IC design technology, including standard-cell and gate-array practices, has too little design leverage to be able to support the market for user-designed chips. Furthermore, what leverage exists is not the most important type. For example, a gate-array methodology that permits a designer to go from a detailed logic diagram to a metalized 2,000-gate complementary-MOS gate array in two weeks does have some layout leverage, but at the expense of silicon efficiency and versatility (many functions cannot be implemented on a gate array). More important, however, is *that this methodology* has had absolutely no effect on the many other time-consuming and error-prone tasks in the total design process, such as logic design, modeling, simulation, or architectural exploration.

With respect to IC design technology as it exists, the position of integrated systems technology and silicon compilation can be described by analogy: if producing an integrated system is akin to arranging transportation between two points, then present design technology is a garage full of automobile parts, some power tools (the equivalent of CAD tools), and an assembly manual. Integrated systems technology is the assembled automobile: the user need merely get in and drive.

Designers needing a VLSI implementation of a system can, with great effort, create a collage of systems from all the component parts in the current IC-design-technology market, and get a fair measure of expertise and methodology. But the vital leverage is missing.

Tower of Babel

The development of integrated systems technology involved creating several models of the classical design process. The most important is the "view" model, which holds that during the design process, the designer creates and maintains several views of his circuit, which include a functional view, a functional simulation view, a logical view, a logic-simulation view, and circuit and circuit-simulation views. It includes also a topological view, and performance, power, and testing views.

Each of the foregoing design views historically has been documented in different formats and has had its own CAD support tools. During the course of the design process, the designer is forced to generate views separately and to translate repeatedly from one view to another. Frequently, such translations are generated manually, with great effort. The major differences between these views, and the lack of standardization of the CAD and computer-aided-engineering tools supporting the views (that is, a nearly total lack of common interfaces), create a Tower of Babel syndrome. The lack of a common base for communications means confusion and fragmentation of purpose. It is also one of the reasons that VLSI design is so difficult, and is practiced by so few persons.

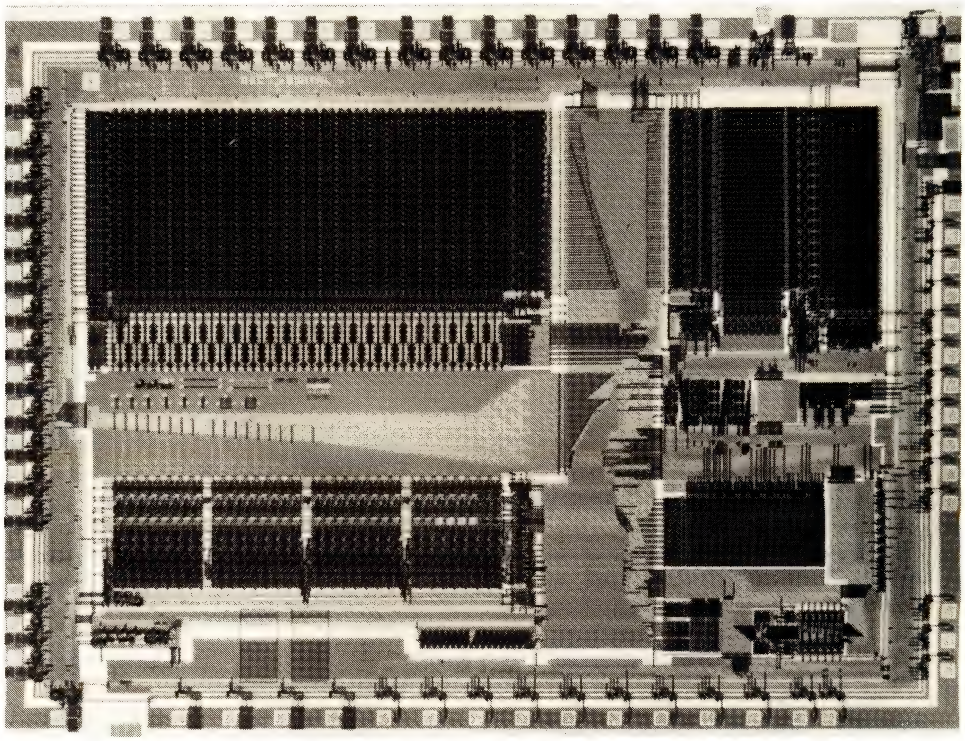
The "complexity" model of VLSI design is depicted in Fig. 2. In the classical, top-down design approach, a 20,000-gate circuit may be composed of 50,000 transistors implemented topologically with over 1 million geometries. Perhaps 2,000 cells (of the complexities associated with standard-cell design) would have been required to implement the 100 or so major blocks from the block diagram. Finally, these 100 blocks were functionally part of about 20 architectural-level modules. The classical designer must manage all of these complexities, at each level (or view) of the design.

Virtually all designers today approach VLSI design by such a top-down, hierarchical decomposition. Unfortunately, a VLSI designer, once having specified a behavioral description of an integrated system and having designed a high-level architectural description (at the block level, or above), must then wallow in logic, circuit, and geometric design, often for years on one chip. Design at higher levels of abstraction implies that the design process may stop at perhaps the architectural (or module) level.

Design leverage

Silicon compilation creates design leverage by keeping the user from having to do any design activity below the leverage line denoted in Fig. 2. That is, all details of VLSI design and implementation below the block level are hidden from, and transparent to, the user by the technology. Design leverage is attained by holding design activity to high levels of abstraction. This management of complexity, in turn, is obtained through design synthesis, the process of automatically creating from the architectural-level circuit description all required views of the circuit and all abstractions below the leverage line.

There are several other important points in the VLSI



1. 64-bit data path. The main engine of the MicroVAX, less its microcode store and control-store sequencer, is a new architecture developed using a silicon compiler. Containing the control decoder, 32-bit arithmetic and logic unit, a 64-bit barrel shifter, 47 dual-port registers, and more, it measures 98,000 square mils.

The application-specific IC market starts to grow

In recent months, industry watchers such as Dataquest Inc. have begun to predict that a revolution is at hand, fueled by moves made by electronics manufacturers to integrate entire systems or major subsystems on single chips. The San Jose, Calif., market-research firm believes that in 1990, application-specific integrated circuits will account for $20.6 billion of a total IC market of $43 billion, up from a 1980 application-specific market of about $2 billion. More significantly, it predicts that nearly 40% of these will be designed by their end users.

The tremendous payoff of system-level integration has already forced scores of systems manufacturers to learn the difficult and arcane arts of IC design and manufacture. Even then, their expertise is typically concentrated in small groups of IC experts, whom the systems designers treat almost as chip vendors. But it is estimated that only about 2,000 people are employed as IC designers, as opposed to approximately 400,000 systems engineers, worldwide. Therefore, most observers believe that this dramatic growth—especially in user-designed chips—will not occur unless there is either a significant change in VLSI design methodology, or introduction of powerful new design-automation tools, or both, so as to enable systems engineers to design cost-effective VLSI. Cost-effective implies design-turnaround time measured in months, effective use of the silicon real estate, and design at only the architectural level.

The market for application-specific ICs is causing two submarkets to appear—the IC-design-technology market and the silicon-foundry market. Suppliers in the design technology market range from small houses that hand-design chips for third parties; vendors of computer-aided-design tools, who supply equipment for various parts of the design process; suppliers of work stations for computer-aided engineering, who initially concentrated on design-documentation entry but now seem inexorably drawn into the CAD arena; and several leading-edge firms concentrating on design automation. Organizations that provide standard-cell libraries, gate-array libraries, and either CAD or design-automation tools for using them are also players.

The silicon-foundry market today is principally served by several merchant-market IC makers who offer standard-cell or gate-array methodologies to customers, and hence are participants in both the IC-design and silicon-foundry markets.

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design process where tremendous leverage can be applied to meet the goal of an integrated systems technology. One of the most obvious and least exploited points in integrated systems design, which can effect a large improvement in the function, performance, quality, or silicon efficiency of a VLSI circuit, is that of the exploration or investigation by the designer of a variety of alternative architectures for a given circuit. Although such exploration is practiced to a small degree today, the process is tedious and inaccurate. Much information that would influence the selection from competing architectures is unavailable until logic design, circuit design, and layout are nearly complete. At this point, the issue of changing architectures is moot. But architectural exploration, when done correctly, can result in final VLSI designs that are significantly more efficient—and hence more cost-effective—than those attainable under the limited exploration typical of classical VLSI design.

Such exploration would be limited without an accurate means of estimating the characteristics of the finished circuit—such features as die size, power dissipation, or critical-path timing. Today, most important features, especially those affecting performance or cost, cannot be determined accurately until layout is essentially complete. The ability to estimate these and other features during architectural exploration means that the trade-offs between competing architectures become clear.

Other design leverage is also manifest. Since IC designers spend a significant amount of time tediously translating each view of the design to the next, such as from the architectural view to the logic view or to the logic-simulation view, a technology that can synthesize all views from one common abstraction will not only reduce time, but will reduce the attendant errors and confusion.

The decoupling of a design from a manufacturing process solves one of the most pervasive problems for users of custom or application-specific VLSI chips—that of ensuring an uninterrupted source of ICs by enabling several fabrication lines or manufacturers to produce the same part. Today, however, the common reality is that for a given chip to run in a manufacturing area (other than the one for which it was designed), often it must be redesigned.

Human creativity

Another vital and completely overlooked area where the design process can be significantly enhanced is that of the design flow itself. The classical design process, even when approached with a standard-cell or gate-array methodology, proceeds monotonically from state to state, from view to view.

Silicon compilation, by contrast, addresses all of the circuit-design views listed above at once. It integrates all ancillary support functions such as simulation and timing verification. But architectural design is left to the human; the designer's creativity has not been replaced.

The table lists the aspects of IC design technology that are accommodated by silicon compilation. Those aspects served by CAD or CAE are also shown. Integrated systems technology, in the true spirit of design automation, automates and integrates virtually every aspect of the design process possible, except those tasks requiring human creativity and judgement.

The compilation philosophy, *which* provides for a compiled layout from an architectural description, has been generalized to include the compilation of all other information germane to the design process, enabling the designer to guarantee that his design can function as desired, within required timing and power constraints.

There is an analogy with software: not only does a software compiler produce assembly code, but it also concurrently produces cross-reference listings, ancillary debugging modules, and, with modern systems, source-code control aids, data-flow diagrams, program hierarchy diagrams, and so forth. All of these items, produced concurrently by the expanded compilation system, are vital to the program-development process. The fact that they are produced concurrently and automatically, rather than asynchronously and manually, gives the programmer vital leverage to optimize his creative work. In addition, clerical work and the Tower of Babel syndrome are eliminated.

In the same manner, silicon compilation provides designers with integrated design, verification, and documentation. Formatting and translation problems between the various tools are eliminated because the compiler is the only tool required. It concurrently synthesizes, from the same architectural description, functional models at all levels in the design hierarchy, functional simulations, timing models, timing simulation, power estimates, and, of course, layouts. Thus nearly all of the important views of a circuit are produced automatically as part of the compilation process. Two additional views, the logic-simulation and circuit-simulation models, are not required with silicon compilation. (The last view, the high-level architectural description, is always left up to the designer's creativity).

New design process

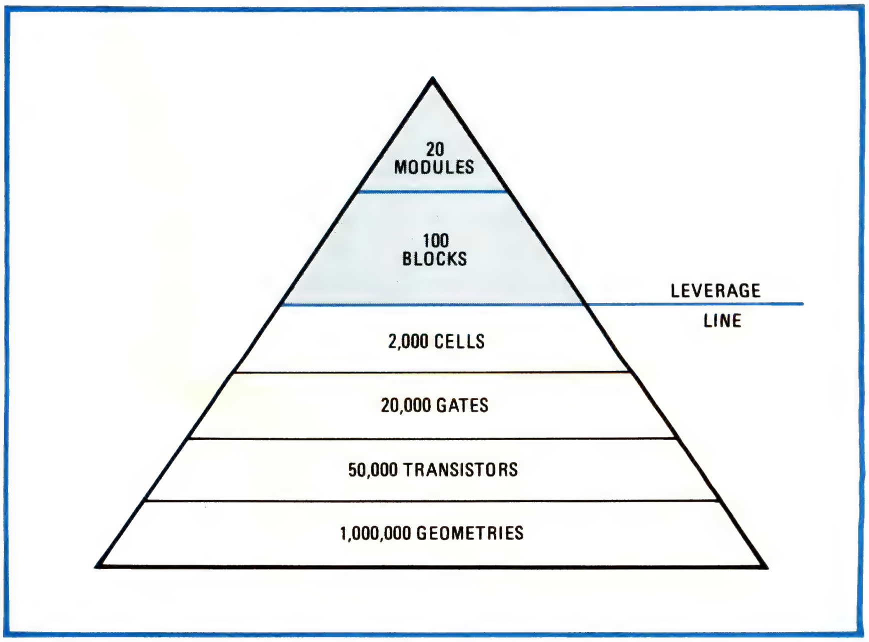
Because of this concurrent nature of the development of each required circuit view, an incremental or successive-refinement approach to design becomes far easier. Incremental design is quite different from the classical sequential VLSI design process, but it is very similar in nature to other mature, creative pursuits of man. For example, an artist, when approaching a new painting, starts with a sketch and slowly refines the entire canvas, adding more color and more detail, until the work is complete. He designs by successive refinement. Integrated systems architecture is also an art, and systems designers are artists as well as engineers.

The compilation process is such that at any point, most of the ultimate characteristics of the finished chip can be estimated from whatever data is available. In practice, this means that as soon as an architectural description of a circuit is provided (consisting of major elements such as ALUs, register files, and programmable logic arrays), the compiler will, upon request, estimate die size and power consumption. The architectural description need not be finalized for this to occur. As additional details are filled in (such as whether the ALU has result registers, and if so, how many), the estimates become more accurate. The compiler will inform the designer when sufficient information has been accumulated so that the next major step may be attempted.

With silicon compilation, the designer can lay out the floor plan long before the total details are known about each of the architectural building blocks. However, when the last detail is actually provided, the user can begin functional simulation (the model having been automatically constructed by the compiler), or begin wiring. Similarly, timing estimates may be obtained before wiring is begun.

As the design is refined, the estimates are improved and updated. The designer provides additional refinement in an incremental fashion, as he determines from the estimate whether he wishes to continue to pursue his current approach. At any time, he may change it. But since the net cumulative investment in design time at any point is so small (hours or days), he is encouraged to continue to experiment until the best architecture emerges and all the architectural refinements are specified. The ultimate refinement is, of course, the finished circuit. The data that is available at this point includes the final layout in a form suitable for pattern generation.

Architectural exploration, which is one of the greatest leverage points in the design cycle, occurs spontaneously. Regardless of the innate ability of any silicon compiler to



2. Top-level leverage. Putting an automated tool to work at a high level in this design-complexity model gives the systems designer with an architectural viewpoint the ability to work with ideas at that level; yet he or she will still have detailed knowledge of the effects of these ideas in terms of the cost and performance of the silicon-based end product.

TABLE: WHERE DESIGN TOOLS ARE USED

IC-design steps	**Computer-aided engineering**	**Computer-aided design**	**Silicon compilation**
Expertise components:			
Intuition			
Creativity			
Experience			X
Discipline			X
Methodology steps:			
Implementation strategies			
Problem breakdown			X
Manpower allocation			X
Toolset selection			X
Analysis limits defined			X
Designer-imposed constraints			X
Design capture	X	X	X
Design style strategies			
Clocking approach			X
Low-level architecture			
High-level architecture			X
Verification strategies			
Circuit modelling			n/r
Logic modelling			X
Stimulation modeling			
Functional verification (simulation)		X	X
Topology verification (design-rule checking)		X	n/r
Modeling for performance verification			X
Performance verification (timing)		X	X
Manufacturing strategies			
Processes			X
Manufacturers			X
Manufacturing preparation:			
Verification/qualification			
Functionality verification (testing)		X	X
Process checking			
Circuit characterization			
Manufacturability qualification			
Manufacturing setup			
Foundry-specific layout additions			X
Test-tape preparation			
Bonding-diagram preparation			X
Layout digitizing		X	n/r
Pattern-generation tape preparation		X	X
Mask preparation			
Manufacturing:			
Fabrication			
Assembly			
Testing			
Documentation	X	X	X

(n/r means this component not required)

produce circuits of a certain density, architectural exploration virtually guarantees that the final circuit will be efficient by comparison with a classically designed circuit. Here, the difference is in the final architecture. In the classical design process, architectural exploration is minimal, because it is so difficult. With silicon compilation as it is today, the mechanics take only a few hours. Virtually all of the designer's time can be spent in the architectural-design phase.

A matter of time

Figure 3 shows the practical results, both the time and the manpower differences for chips at the 40,000-transistor level. The times from the classical design process do not scale to the silicon-compilation example. Rather, the designer ends up spending more time on other pursuits, such as architectural exploration, than he did in the classical process.

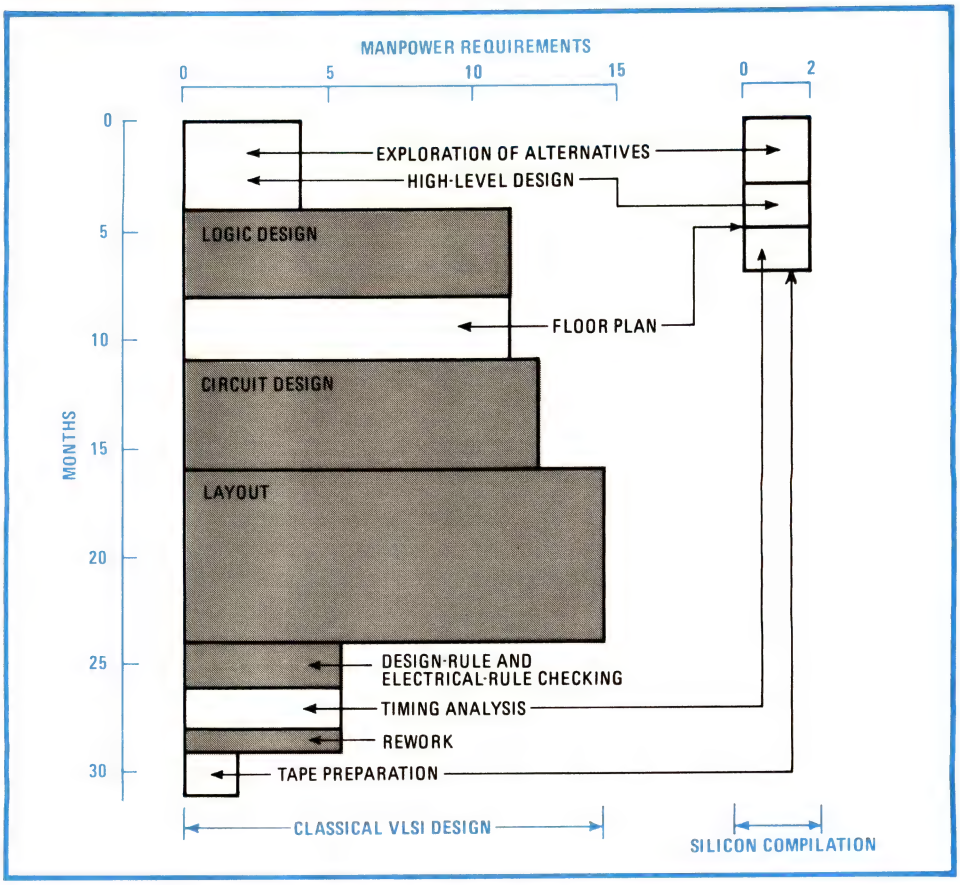
Silicon Compilers undertook several custom chip-design projects designed to wring out the silicon compilation process. The Ethernet data-link controller project, begun shortly after the firm's founding in 1981, took a total of eight months, with the first three consumed by architectural exploration. This phase culminated in a chip specification, which was then implemented using a prototype silicon compiler in the remaining five months. A significant portion of this time was consumed by the development of the compiler itself. Two engineers were required for the chip architecture and implementation, while the development of the compiler took the remainder of the company's resources.

The resultant chip, which is being manufactured under license from Silicon Compilers, was implemented in a 3-micrometer n-MOS process (Fig. 4).

Input to the compiler was an eight-page high-level description of the circuit written in a proprietary architectural-description language. Among the blocks synthesized by the compiler are two programmable logic arrays, a first-in, first-out buffer, three data-path blocks (registers, comparators, counters, and zero-detection logic), a serial data path, clock generators, a linear-feedback shift register, bonding pads, and assorted random logic. The floor plan was laid out interactively, which the company prefers for architectures containing less than 100 blocks. Interconnection was accomplished with the compiler's intrinsic router.

Rapid turnaround

The second project was a proprietary circuit for bit-mapped-graphics operations. Called the RasterOp Controller (Fig. 5), it was designed for Sun Microsystems of Santa Clara, Calif.,' for use in their line of work-station products and has been well received by Sun, according to Andrew Bechtolsheim, who is vice president of technol-



3. Comparing outlays. A comparison of the time and effort put into various phases of IC design as it is generally practiced versus current work levels for Silicon Compilers Inc. at the 40,000-device level includes the use of computer-aided-design and -engineering tools, which have reduced the size of some of these blocks a certain percentage. Silicon compilation leaves the designers in the architectural phase even longer, but then truncates the process, making logic and circuit design, layout, and electrical-rule and design-rule checking unnecessary.

ogy. The entire design required only one engineer working five months.

The rapid turnaround of the MicroVAX I data-path chip was a key element in DEC's strategy to complete the design and implementation of the MicroVAX within one year. Silicon Compilers worked in concert with a VAX design team from Digital's Belleview, Wash., facility (DEC West).

The partitioning of the design into the ROM microcode store, control-store sequencer, and the data-path chip was considered optimum, since it kept the latter chip at a reasonable size and took advantage of the proven, high-density ROM technology. From a project-management standpoint, it permitted DEC West to concentrate on the microcode development for the VAX instruction set, while the compiler was applied to the data-path chip itself. Finally, it offered a simple way of implementing last-minute changes in the microcode.

The internal architecture of the data-path chip was totally new. Although systems manufacturers often attempt to reduce costs by reimplementing old architecture in a new technology, as is often done today with gate arrays, such an approach is usually not optimal, since many of the original trade-offs do not hold for the new technology. Instead, as was the case with the MicroVAX chip, a totally new architecture is more appropriate.

The silicon-compilation technology has already been expanded to provide automatic synthesis of new blocks required for the chip. The IC carries RAM, ROM, a timer, a counter, random logic, programmed logic arrays (inhibit and ALU-decoding logic), and a multiplexer for operand logic, in addition to the 32-bit ALU and 64-bit barrel shifter mentioned earlier.

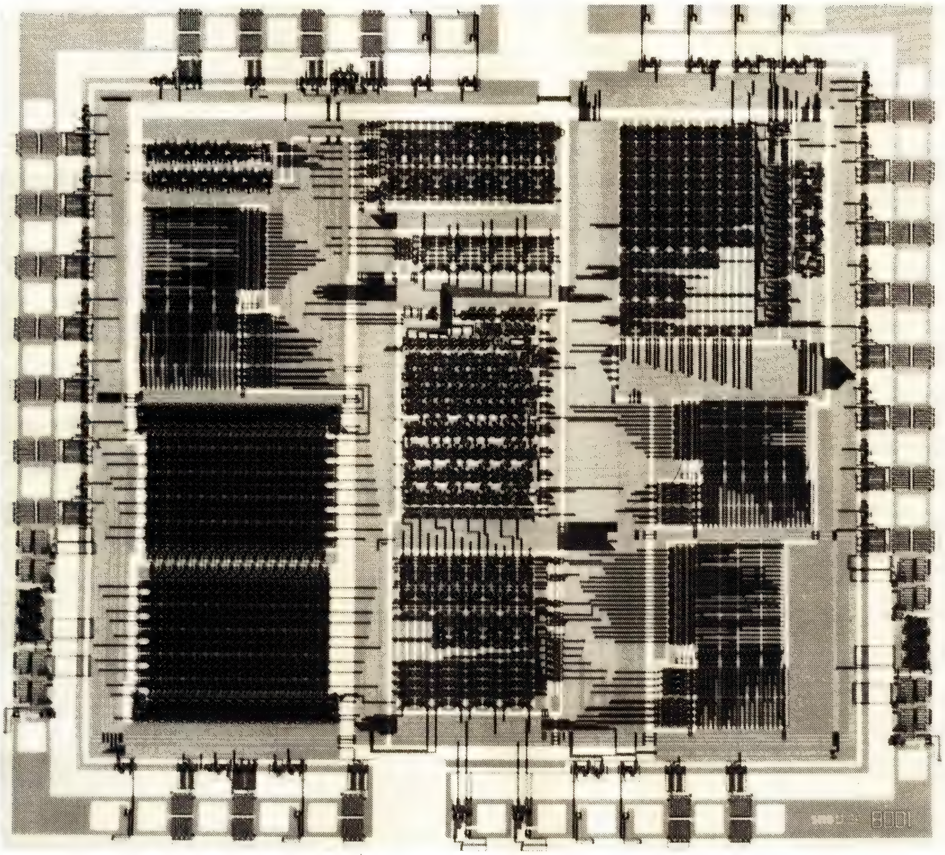
Since silicon compilation synthesizes large blocks automatically, one of the major challenges in its development is to guarantee that every single possible combination of user-specified options for a given block type generates electrically and topologically correct layouts. To this end, traditional CAD and CAE tools, used to verify the construction and operation of the silicon compiler, and including gate-level simulation, circuit verification, design-rule checking, network analysis, and engineering-change control, have been considerably enhanced.

Functional correctness of the data-path chip was guaranteed by an extensive simulation effort, with both firms involved. Simulators built by each team were run with identical sets of test data until both the simulators and the design converged. Silicon Compilers concentrated on simulation at the functional level by generating models that predicted the performance of each of the blocks. Simulation models are now automatically synthesized at the same time as the block layouts.

Slow to catch on

The performance of the MicroVAX chip was guaranteed by static-timing analysis. Timing models are now also automatically generated for each block, and for an entire chip, or any partitioning. An integral static-timing verifier then yields timing reports indicating critical paths, maximum clock frequency, setup and hold times, and other such performance-related data.

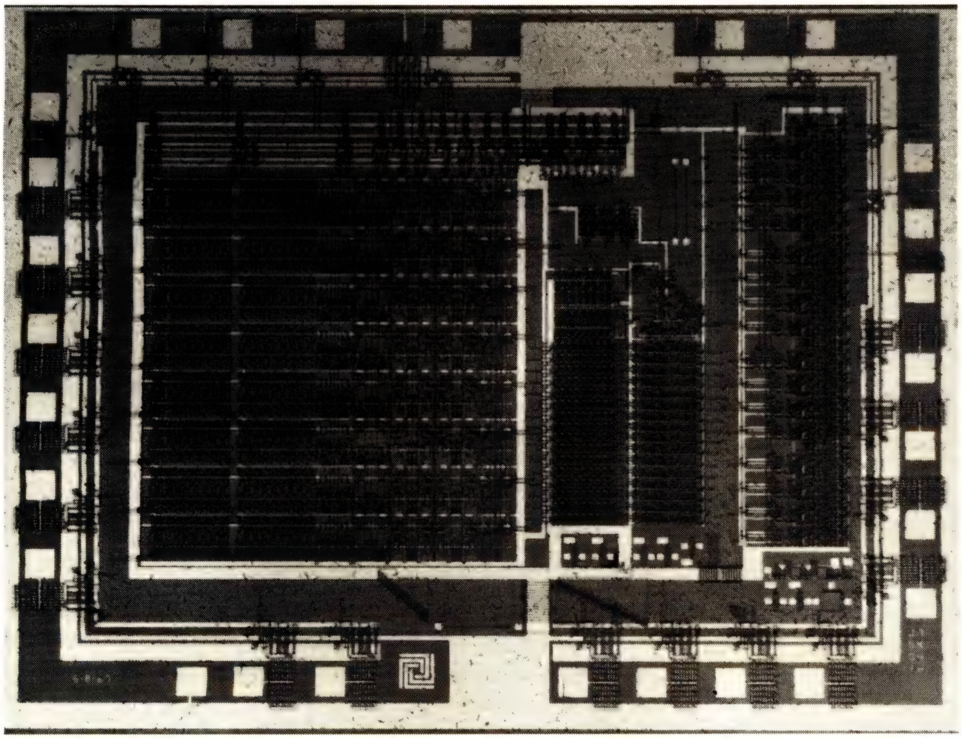
If silicon compilation were simply to become a tool



4. First project. The Ethernet data-link controller, built in a 3-micrometer n-channel MOS process, was designed with a prototype compiler during the design phase of the current silicon compiler. The floor plan was laid out interactively, which is preferred for parts with less than 100 blocks.

used by today's VLSI designers, it would fall far short of its ultimate goal, which is to make it possible for the hundreds of thousands of competent systems designers in the electronics industry today to begin designing integrated systems at the VLSI level. The benefits of integration are so great that many electronics manufacturers are beginning to view silicon compilation as the most important single breakthrough in IC design technology in this decade.

Until now, however, silicon compilation has failed to capture the imagination of much of the IC design community. Many pundits have claimed that silicon compilation's ultimate manifestation includes automatic architecture—that is, silicon output given no more than a behavioral description. As a result, many IC designers who already know better end up dismissing silicon compilation out of hand. Others fear it the way an assembly-line worker fears the coming of robots. But in reality, the production silicon compiler such as has now been developed greatly simplifies the job and would captivate the most conservative IC designer today. ☐



5. Graphics chip. The RasterOp controller for high-performance bit-mapped graphics was designed for Sun Microsystems Inc.'s work stations by a single engineer working only five months, using silicon compilation. The MOS part measures 182 by 151 mils in a 3-micrometer high-performance process.

Modular approach to C-MOS technology tailors process to application

Despite the proliferation of applications, a few C-MOS process variations can address the functional requirements of many different products

by Kim Kokkonen and Richard Pashley, *Intel Corp., Santa Clara, Calif.*

☐ In the past few years, the interest in complementary-MOS technology and its applications to new products has exploded. Traditional arguments for C-MOS center on its low power dissipation, the large noise margins of complementary logic, and its simple ratioless design. With the advent of very large-scale integration, these arguments are taking on new meaning and importance.

As an example, Fig. 1 compares the performance of H-MOS (high-performance n-channel MOS) inverters with their equivalent in Intel's C-H-MOS (complementary high-performance MOS) technology. Though H-MOS's speed continues to improve with further scaling, its delay-power product is more than an order of magnitude higher than a C-H-MOS implementation with identical n-channel transistors. In a VLSI part with 50,000 gates, C-H-MOS could mean the difference between 1 and 10 watts of power dissipation, which might save the expense and difficulty of a sophisticated cooling system or extend a portable system's operating time by a factor of 10.

That C-MOS performance is now on a par with n-MOS technology has also accelerated its popularity. In addition, the density of C-MOS circuitry has improved dramatically with advances in technology. Finally, the number of process alternatives has grown so large that almost any integrated-circuit design can be supported with available C-MOS technology.

Unfortunately, the wave of enthusiasm for C-MOS and the needs of different applications have multiplied the number of approaches that C-MOS developers are taking. Several major issues remain in VLSI C-MOS design—namely latchup and soft-error prevention, interconnections, and logic-design techniques. A building-block approach with a limited number of basic process modules can be used to create a close-knit family of technologies that squarely addresses these issues and simultaneously supports a wide range of applications.

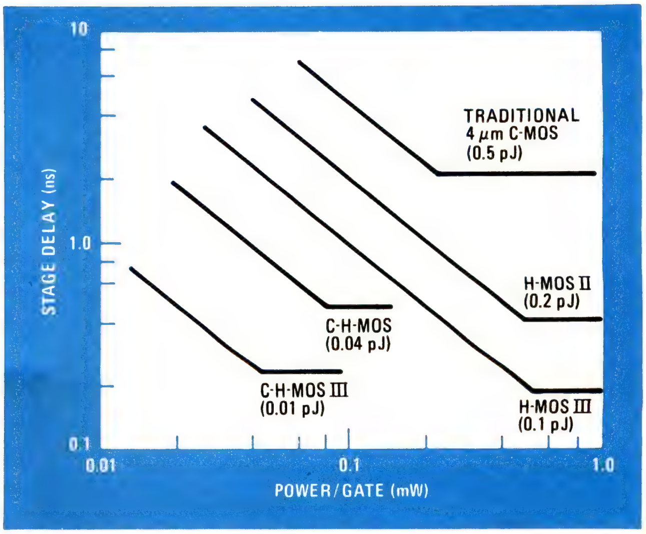
The basis for C-H-MOS

A firm foundation in n-MOS-transistor physics will support the advancement of C-MOS technology. As channel lengths approach 1 micrometer, n-channel transistors become more difficult to optimize because the standard 5-volt power supply causes problems with high-intensity fields. Improperly designed transistors may be unreliable as a result of hot-carrier injection into gate oxides, or they may cause less localized problems by injecting carriers into the MOS substrate—there to bleed charge from storage nodes or even trigger a destructive latchup.

The resources to develop and verify the reliability of a 1-μm n-channel transistor are well established and substantial. In Intel's C-H-MOS process, the basic design of the n-channel transistor is identical to its H-MOS counterpart, as shown in the table. Even at the more detailed levels of doping profiles, the H-MOS and C-H-MOS transistors are nearly identical.

Thus a high-performance C-MOS technology may be born out of an established n-MOS line. The relatively simple addition of an n-well in the same high-resistivity substrate results in a C-MOS process that serves as the basis for several optimized technologies. This is just a start, however, as other important issues remain.

Latchup has been the traditional nemesis of C-MOS. Given the presence of parasitic silicon controlled rectifiers within every bulk C-MOS chip, a current pulse of sufficient magnitude either inside or outside the chip may cause a catastrophic latchup. Many schemes have been proposed to combat latchup, ranging from carefully scrutinizing the layout (which imposes no burden on the technology) to a buried layer (which significantly in-



1. Power down. Despite the continuous improvement of H-MOS (high-performance MOS) by scaling, the delay-power product for C-H-MOS (complementary-MOS H-MOS) is more than an order of magnitude lower in the typical integrated circuit.

n-CHANNEL TRANSISTOR COMPARISON

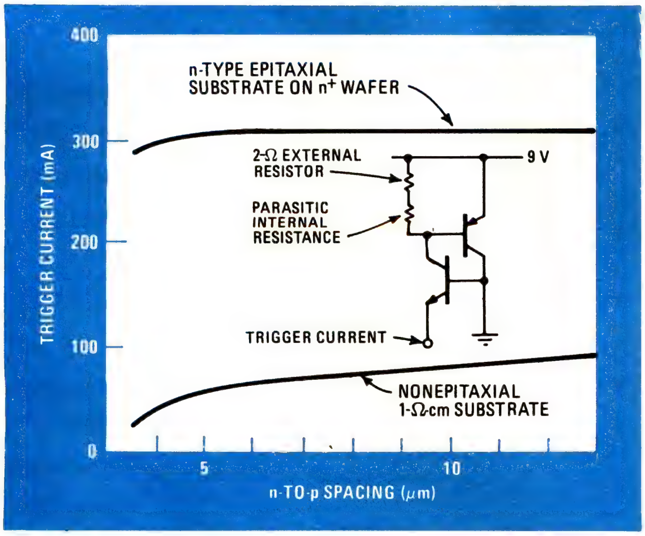
Technology		Gate-oxide thickness (Å)	Channel length (μm)	Threshold voltage (V)	Graded drain profile
n-MOS	C-MOS				
H-MOS I	—	700	3.0	0.7	no
H-MOS II	C-H-MOS	400	2.0	0.7	no
H-MOS II	C-H-MOS III	250	1.0	0.7	yes

creases complexity and processing cost). All have some degree of effectiveness.

A modular approach to a broad-based line of C-MOS technologies requires other measures besides mere physical latchup resistance. The latchup spoiler must be applicable to dynamic random-access memories, erasable programmable ready-only memories, and static RAMs, as well as to microprocessors and controllers. In order to improve latchup resistance, it cannot increase the distance between n- and p-channel transistors (this constraint is most significant in random logic and full C-MOS six-transistor static-RAM cells). The technique must be compatible with low-cost and large-volume manufacturing. Finally, the approach must be consistent with the use of an automated checking algorithm, so that every gate of a large semirandom logic design need not be scrutinized for latchup susceptibility.

Epitaxial benefits

Figure 2 shows the margin gained in latchup trigger current when an epitaxial substrate is used. The epitaxial substrate brings the same latchup benefits to all product lines, and in many cases provides additional advantages such as improved surface lifetimes (for dynamic RAMs) and reduced dc resistance (for E-PROMs and logic). Epitaxial substrates are now available in volume from commercial silicon vendors, adding less than 5% to the cost of a finished wafer. No additional or exotic fabrication equipment needs to be installed. Because the epitaxial substrate's heavily doped bulk effectively eliminates the vertically triggered latchup mode, it is possible to develop a set of computer-aided-design tools that can flag latchup-sensitive layouts on the largest VLSI chips.



2. Benefits. By raising the margin of latchup trigger current, an epitaxial substrate effects a dramatic improvement in combatting latchup, a major concern in complementary-MOS chip design.

Since grasping the phenomenon of upsets induced by alpha particles, in 1977, memory designers have taken care to ensure that enough charge is stored within each cell to minimize the problem. As critical chip dimensions are reduced, this problem becomes more severe, however, since both parasitic and storage capacitances are naturally reduced. For the latest 1.5-μm n-MOS process, stored charge is low enough to caution even microprocessor designers to guard against random storage nodes suffering from soft errors. Fortunately, C-MOS provides a natural barrier against soft errors if the storage node is located within the C-MOS well.

The well junction is reverse-biased by the power-supply voltage. The electric field at this junction naturally repels any carriers generated outside the well that might otherwise diffuse up to surface storage nodes. The combination of the well structure and an epitaxial substrate is even more effective. Here the funneling mechanism that usually collapses local electric fields during the passage of an alpha particle is also minimized. By using epitaxial substrates and the protection of a C-MOS well, the amount of charge collected during an alpha event can be reduced by an order of magnitude.

Of course, the designer must arrange for the storage node to reside within the well. This constraint, combined with other performance issues, leads to different choices of well and substrate polarities, depending on application. For example, in a C-MOS technology that is optimized for dynamic RAM, the ideal memory cell should have a p-channel pass gate and a p-channel capacitor located within an n-well in a p-type substrate. The p-channel transistor is chosen because it injects far fewer spurious carriers into the substrate and thus does not by itself disturb the state of neighboring cells.

The conductance of the p-channel device, while lower than that of an n-channel device of the same size, does not degrade the RAM's performance, since dynamic-RAM sensing is limited primarily by the amount of stored charge. Experimental results with C-H-MOS dynamic RAMs based on these principles show a soft-error rate of less than 300 FIT (failures in time, or device failures per billion hours) at a power supply of only 3 V. This is an improvement of more than three orders of magnitude over traditional n-MOS dynamic-RAM technology and offers the possibility of dynamic-RAM systems that require no error correction and that are compatible with low-voltage battery backup.

High-density, high-performance static RAMs present the other side of the coin. The smallest static-RAM cells today are built using polysilicon-load resistors that sustain the stored-node voltage. On the time scale of an alpha event, however, these resistors in effect do not exist. Because the storage node's RC time constant is on the order of milliseconds and the alpha event's time scale is nanoseconds, the cell appears dynamic. In this sense, polysilicon-load static-RAM cells are very similar to dynamic-RAM cells. The major difference arises in the way the cells sense the cell's information. The static-RAM cell provides a direct current, and to maximize the cell's performance, that current must be as large as possible while contained in a minimum area. Thus the chip designer must use high-gain n-channel transistors for the cell's pass gates and pulldowns. For good soft-error protection, then, the cell must be located in a p-well within an n-type substrate.

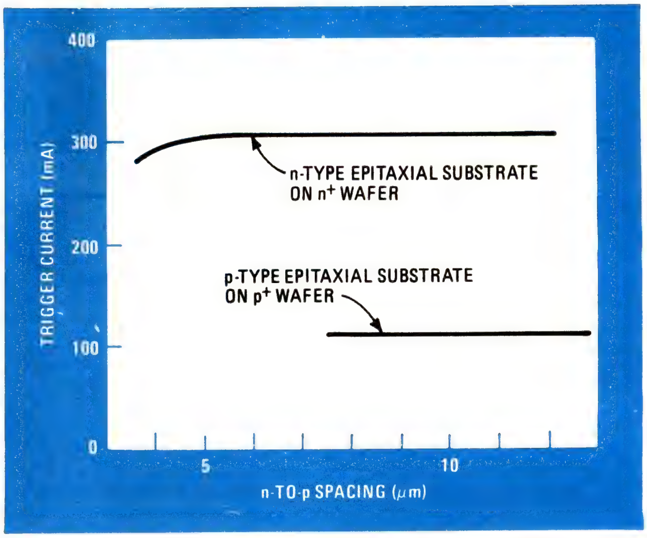
The p-well approach benefits even full C-MOS six-transistor static-RAM cells. The area of such cells depends strongly on the distance allowed between n- and p-channel devices. Using a straightforward implementation of epitaxial C-MOS, the p-well approach provides more margin against latchup at small n-to-p spacings (Fig. 3). This phenomenon occurs because of the differing diffusion properties of n- and p-type dopants. The heavy doping in the n-type substrate is less mobile than is the p-type dopant, resulting in less outdiffusion during thermal processing and thus minimizing the shunt resistance that controls latchup.

Hooking it up

One of the challenges of C-MOS in logic applications is interconnection. Designers of n-MOS chips are accustomed to buried contacts, which directly connect n-type polysilicon and n-type transistor source or drain regions. Because C-MOS requires contact to both p and n regions, the traditional n-type buried contact becomes much less useful, and a version suitable for both diffusion polarities is quite difficult to implement. This increases the burden on contact and metallization modules.

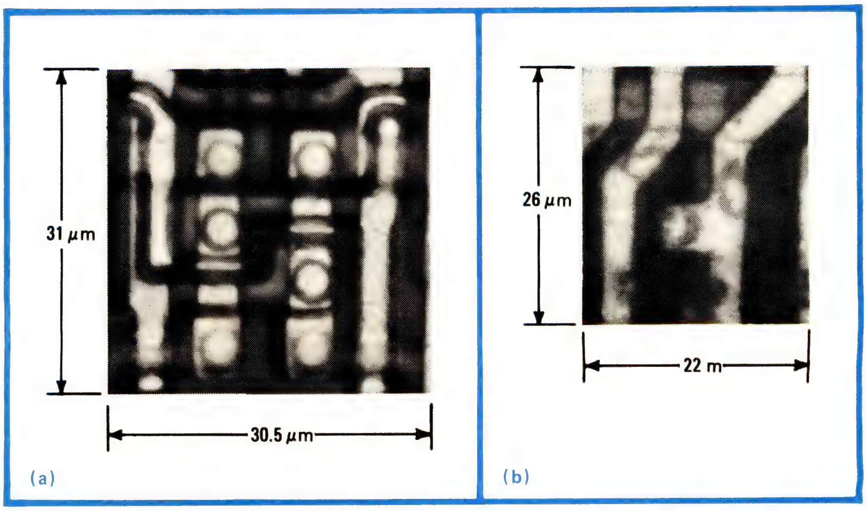
For high-density C-MOS logic, the first level of metal is all but consumed by local connections between p and n transistors. The payback from adding a second level of metal for longer-distance routing is very high. A good example exists for the six-transistor static-RAM cell commonly used by logic designers. Figure 4 compares single- and double-metal versions of this cell, both implemented with 1.5-μm design rules. Here the second-metal layer provides the bit lines for the cell. Similar arguments justify the use of second metal in global power, clock, and data routing in complex microprocessor chips.

Contacts themselves are more difficult to build in C-MOS. N-MOS technology accustomed process engineers to adding a phosphorus contact plug after the contacts have been etched. This plug brought several advantages: the phosphorus gettered metallic contaminants from the wafer, reducing junction leakage; and the high-temperature diffusion rounded the profile of the contact sidewall, easing the step coverage of the metal subsequently deposited. Further, the plug had self-aligning features. If the contact etch attacked the silicon substrate or if the contact was misaligned toward the field-oxide edge, the plug would rejuvenate the resulting weakened junctions. In C-MOS, these same attributes must be obtained differently, through improved fabrication, cleanliness, new gettering techniques, improved dielectrics, and tightly controlled contact etching. Figure 5 shows the difference in implementing a 1.5-μm contact structure in n-MOS and C-MOS.

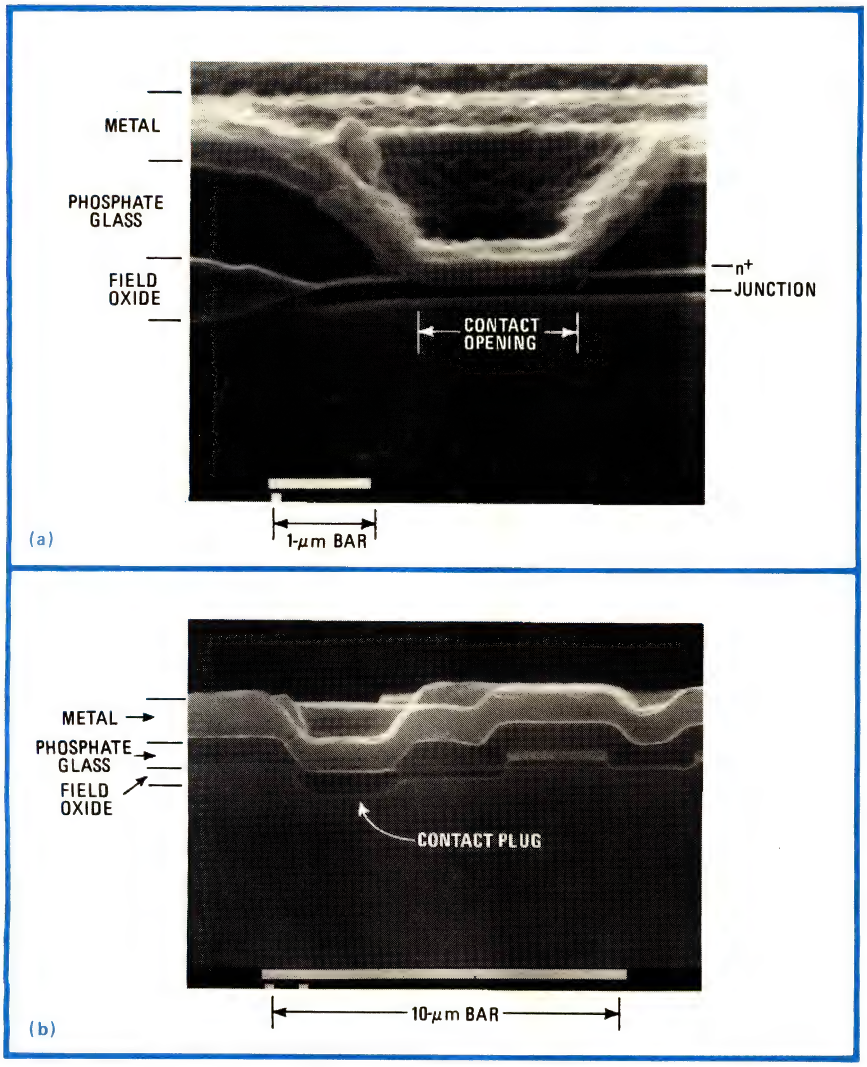


3. P-well margin. With an epitaxial substrate, a p-well structure (upper curve) yields a greater margin against latchup than n-well at smaller n- and p-device spacings.

Along with the proliferation of C-MOS technologies has come a wave of innovation in C-MOS design techniques. For digital logic, the major contenders for broad use are full complementary design and domino logic, first proposed by AT&T Bell Laboratories (Fig. 6). For many applications, traditional C-MOS logic is a winner. It requires no clocks, has larger operating margins, and uses fewer transistors for simple gates. For more complex gates, however, domino logic uses fewer transistors and runs faster. The speed results from connecting fewer transistors in series and reducing gate-fanout loading by



4. Payback. The use of double-metal layers for a six-transistor static-RAM cell can produce a large savings in real-estate. In two cells implemented with a 1.5-μm design rules, the savings can amount to one third of the total area. The cell at right uses second-layer metal for bit lines.



5. Making contact. Contacts are more difficult to build in C-MOS than in conventional n-MOS. The phosphorous contact plug used in n-MOS after contact etching (a) adds desirable features such as reduced junction leakage and improved step coverage by the metal layer. To gain the same advantages in C-MOS requires greater process control (b).

up to a factor of two compared with full C-MOS.

Interestingly, the choice of design style influences the optimal type of C-MOS well. The speed of full C-MOS is limited by the slower of the two transistor polarities. Since the trip point is quite close to half the power supply, the time required for either transistor type to discharge its load capacitance by about 2.5 V sets the gate's speed. Since the p-channel device is the weaker one, it pays to choose a well type that improves the p-channel's conductance. P-well does this because the p-device is fabricated in an uncompensated substrate and thus has maximum mobility. Comparisons between n- and p-well construction show that the p-channel's conductance may be improved by as much as 10% with the proper well type.

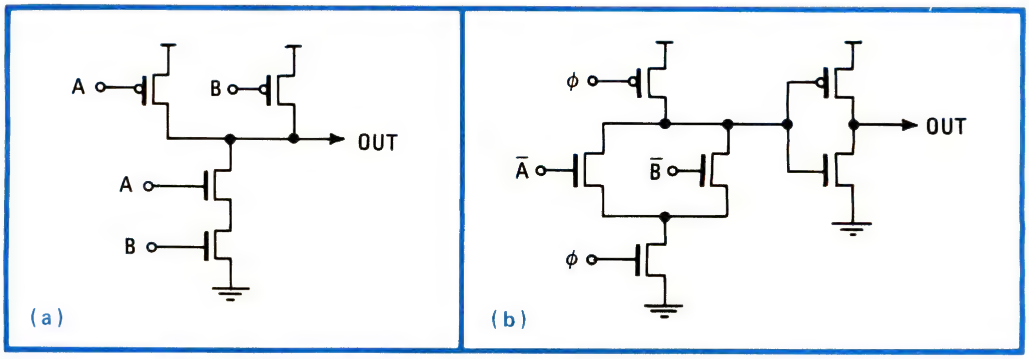
By contrast, domino logic is at its best in an n-well technology. Here, the n-channel transistor dominates both performance and transistor count. Placing the n-channel device outside the well improves its conductance and reduces the dominant parasitic junction capacitance. Density also increases because no well contacts are required for the majority of the transistors.

The twin-well approach to C-MOS blurs these distinctions. In this approach, a high-resistivity epitaxial layer is grown on a heavily doped starting wafer. Then the doping for each transistor polarity may be independently optimized without need for doping compensation. Performance arguments based on mobility or junction capacitance thus become moot. Nonetheless, domino logic will still be best on a p-type substrate (equivalent to n-well) because it does not require well contacts to collect the large parasitic substrate currents from the n-channel transistors, thus improving packing density.

Matching process to product

These and other technical arguments may be combined into a consistent strategy (Fig. 7) for creating a line of C-MOS processes serving a broad marketplace. For at least the next several years, a complete technology line must include C-MOS based on both p- and n-type substrates. Fortunately, choosing epitaxial-latchup control minimizes the development cost of running both process-

6. Logic. Two major contenders for digital logic design are full complementary (a) and domino logic (b). The former requires no clocks and is simpler for many applications. Domino logic, which performs best in an n-well technology, is faster and simpler for more complex circuits.



es. Dynamic RAMs are supported on the n-well side to minimize pattern sensitivities induced by substrate currents while protecting the p-channel cell from soft errors. E-PROMs are built in a similar n-well C-H-MOS process. Placing Intel's n-MOS E-PROM cell in an epitaxial p-type substrate eliminates parasitic effects caused by high substrate currents flowing during cell programming.

Microcontrollers land on the n-well side also, so that they may incorporate on-chip E-PROM cells. Most microcontroller products come in two versions, one with on-chip E-PROM for system-development and manufacturing flexibility, and another with on-chip ROM for lowest cost. Using n-well C-MOS, a single core design can support both versions. Telecommunications and signal-processing products can also take advantage of the n-well E-PROM process, both for its high-quality polysilicon-polysilicon capacitors and for the E-PROM cell's programmable features. High-performance static RAMs, whether six-transistor or polysilicon-load, can take advantage of a p-well C-H-MOS process. High-end microprocessors can key off the dense n-to-p packing and double-metal capability offered by the six-transistor static-RAM process.

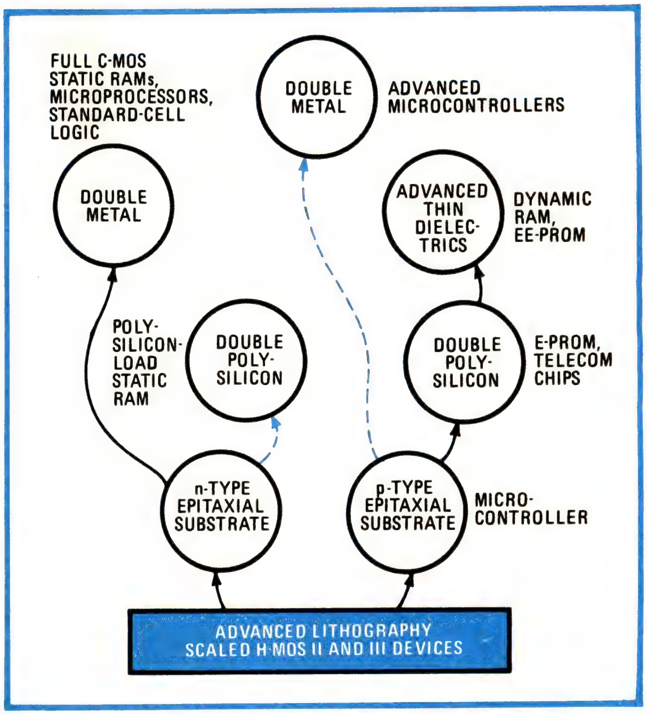
Because these processes are modular, development is simplified and manufacturing overhead is minimized. Just as all the 1.5-μm C-H-MOS III technologies share a common transistor module, the difficult contact module was developed once to be shared among all. Specialized features such as double polysilicon or double metal are extensions of the common base.

The future

C-MOS technology is still developing at a frenetic pace. Surprisingly, the application of some newer techniques and the demands of next-generation circuits may bring the various forms of C-MOS closer together, rather than further splitting the number of integrated processes.

One example of this trend is the development of a trench-isolation technique for separating n and p devices. When this module is perfected, there will be no reason to develop six-transistor static-RAM cells on p-well technology. The near-ideal trench isolation will prevent latchup on either substrate type. Similarly, if stacked C-MOS static-RAM cells can be perfected, there will be no need for polysilicon loads. The stacked C-MOS cell will have the same density but with improved performance and soft-error immunity. At that time, twin-well C-MOS on a p-type substrate, augmented by specialized features for specific product lines, will become the one approach to a broad line of C-MOS processes.

Another factor affecting future C-MOS integration is the continued scaling of transistors. It is well known that the weaker p-channel transistor is gradually catching up on the n-channel device as channel lengths enter the submicrometer region. Eventually, the performance differences may become so small that p- and n-channel devices will be used interchangeably. Before this level is reached, however, the 5-V power-supply standard must be reduced. Because of the large base of TTL-compatible designs and the impossibility of converting the world to a new standard overnight, components operating from the new reduced supply will need to maintain TTL compatibility and also be able to operate in a system that mixes older 5-V components with lower-voltage ones. An on-chip 5-to-3-V converter may be one way to solve the problem. This technique, however, will waste up to 40% of the total chip power within the voltage regulator.


FULL C-MOS STATIC RAMs, MICROPROCESSORS, STANDARD-CELL LOGIC
DOUBLE METAL
ADVANCED MICROCONTROLLERS
DOUBLE METAL
ADVANCED THIN DIELEC-TRICS
DYNAMIC RAM, EE-PROM
POLY-SILICON-LOAD STATIC RAM
DOUBLE POLY-SILICON
DOUBLE POLY-SILICON
E-PROM, TELECOM CHIPS
n-TYPE EPITAXIAL SUBSTRATE
p-TYPE EPITAXIAL SUBSTRATE
MICRO-CONTROLLER
ADVANCED LITHOGRAPHY SCALED H-MOS II AND III DEVICES

7. Technology tree. A relatively small line of C-MOS process variations, or modules, can be matched to a wide variety of products to serve a broad marketplace. The broken lines indicate directions of potential future growth.

C-MOS technology provides an elegant solution because it can drive TTL-compatible output levels from a system power supply as low as 3 V. Since TTL levels are referenced to the negative (ground) rail, the grounded substrate offered by n-well C-MOS is a much-preferred means of integrating submicrometer transistors into such a system. This will be a strong motive to standardize on p-substrate C-MOS.

A final factor that tends to drive future C-MOS processes toward commonality is the growing importance of RC delays in overall chip performance. The latest high-performance static RAMs use an aluminum strap in parallel with the polysilicon word line because the RC delay induced by even the best refractory metal polycides is several nanoseconds too long. Studies of dynamic RAMs larger than 1 megabit similarly indicate that refractory word lines will probably be inadequate, forcing the technology to support two layers of metal. Combining these observations with those made previously regarding the evolution of static-RAM cells leads to the conclusion that most future C-MOS technologies will have two layers of polysilicon as well as two layers of metal.

The development of silicon-on-insulator technology is the one major factor that could renew the divergence of C-MOS approaches in the future. However, until the quality of SOI substrates is adequate to support dynamic RAM and E-PROM cells, and not just static logic, it will not play a major role in a broad-based and modular technology strategy. ☐

Electronic Components Conference to spotlight advances in materials

New ceramic substrates, polyimide-copper systems, and an elastomeric socket for a fine-pitch chip-carrier are features of the sessions in New Orleans

by Jerry Lyman, *Packaging & Production Editor*

☐ Packaging and interconnection have lately come to dominate the topics of papers delivered at the annual Electronic Components Conference, and this year is no exception, at the 34th conference, to be held in New Orleans, May 14–16. Moreover, many of this year's most interesting papers will be discussing packaging materials as well.

For example, there are papers on two new ceramic substrate materials; two high-density multichip packages based on thin polyimide layers on ceramic; a special plastic package that resists cracking caused by the thermal shock in soldering dual in-line packages; an elastomeric connector for a 132-pad fine-pitch leadless ceramic chip-carrier; and connectors with contacts that have a memory for their original shapes.

Alternate ceramics

Alumina traditionally has been the choice for thick- and thin-film substrates, integrated-circuit substrates, and large multichip packages that dissipate considerable power. However, it has some deficiencies, such as its relatively high thermal conductivity and its poor thermal-coefficient-of-expansion (TCE) match with silicon. Two papers from Japan and the U. S. consider ceramics for electronic-packaging applications.

A group of authors from the Large-Scale Integration Research and Development Laboratory of Mitsubishi Electric Corp., Hyogo, Japan, will discuss a flip-chip package that is free from thermal stress. Led by Masanobu Kohara, the authors will point out that for a reliable flip-chip package, one of the most critical problems to be dealt with is fatigue caused by thermal stress. This stems from the mismatch between the TCE of the chip and the package. Mitsubishi's solution is an experimental package using silicon carbide with a fine-pattern circuit of thin-film conductors. The material's characteristics are listed in the table, along with those of several other ceramic substrate materials mentioned below.

Silicon carbide's TCE matches that of silicon very closely, making it suitable as a package for flip-chip devices. However, it is difficult to make the package substrate with the standard cofired ceramic technology combined with thick-film patterning. Instead, the Japanese researchers went to thin-film technology.

The unit (Fig. 1) is 42 by 37 millimeters and has 208 input/output pins. The metalized layers consist of 80 nanometers of chromium for the top layer, 1.2 nm of copper in the middle, and 50 nm of chromium for the bottom layer. Circuit conductors and spaces are at least 30 micrometers wide.

Comparative heat-cycling tests on SiC and alumina oxide packages were run at –50°C to 125°C at 1 cycle per hour. The SiC package survived many more cycles without a joint failure. In addition, the thermal resistance between junction and package of the SiC unit was 1°C/watt lower than that of the alumina unit.

Another alternative to alumina is considered in a paper on alumina nitride by Waltraud Werdecker and Fritz Aldinger of W. C. Heraeus GmbH, Hanau, West Germany. Here the emphasis is on substrates for high-powered applications such as laser diodes, power ICs, and high-speed logic.

Formerly, the only substrate material possessing the thermal conductivity and high electrical resistance necessary for high-power semiconductors was beryllium oxide. However, the toxicity of BeO dust often restricts its use. Therefore, Heraeus has developed an alumina-nitride ceramic that not only has good thermal conductivity and high specific resistivity, but also has a TCE approximately matching that of silicon.

SUBSTRATE PROPERTIES IMPORTANT FOR HIGH-POWER APPLICATIONS

Materials	Thermal conductivity at room temperature (W/meter kelvin)	Electrical resistivity at room temperature (Ω/cm)	Coefficient of thermal expansion for 20°–100°C range (ppm/°C)
$A\ell N$	140–170	$>10^{11}$	2.6
$A\ell_2O_3$	10–35	$>10^{14}$	5.5
BeO	150–250	$10^{13}-10^{15}$	6.5
SiC	90	>5	3.7
Si_3N_4	10–40	10^9	3.1
SiO_2	0.1	10^{18}	0.5

Alumina nitride has some unique properties that assure it of future widespread applications, according to the authors. These include high thermal conductivity, high dielectric strength over a wide temperature range, relatively low dielectric losses at high frequencies, good resistance to thermal shock, good mechanical properties, and low toxicity. Because of the last two factors, AlN can be cut, lapped, polished, and drilled in the same manner as aluminum oxide.

Polyimide, a high-temperature polymer frequently used as a laminate for rigid and flexible printed-circuit boards, is gradually finding more use as an insulating layer in multilayer ceramic substrates and even in IC processing, as several papers will show. The Musashino Electrical Communications Laboratory of Nippon Telegraph & Telephone Public Corp., Tokyo, and the Honeywell Corporate Technology Center, Minneapolis, each will present papers on high-performance multichip packages based on layers of polyimide with copper conductors built up over an alumina base.

Polyimide options

The Musashino paper, by Kunio Moriya and two colleagues, describes a multilayer ceramic structure built up by forming fine copper patterns and via holes on photosensitive polyimide layers. This process starts with spin coating of the photosensitive prepolymer solution. Then via holes are formed by photolithographic and chemical procedures. Next the polyimide is hard-cured and conductors are electroplated on.

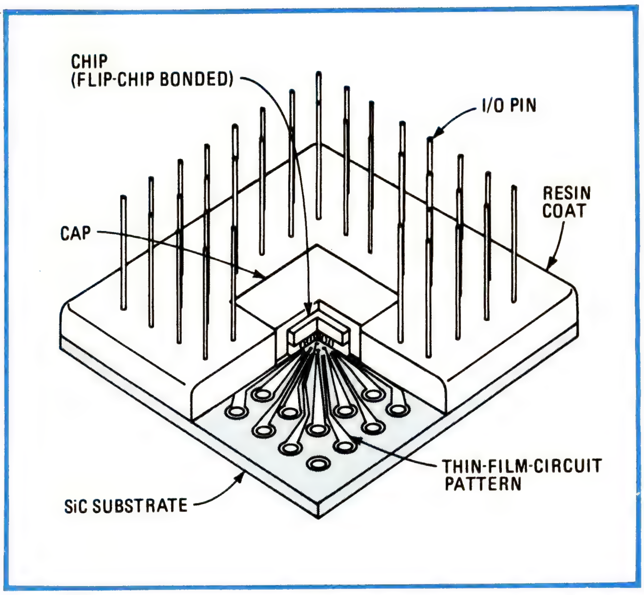
With this process, the Japanese firm's engineers have fabricated an experimental four-layer interconnection to evaluate processing techniques. This unit has four conductive layers each 3 μm thick and three dielectric layers each 10 μm thick. The conductive pattern has 10-μm-wide conductors and 20-μm via-hole diameters. Tests have proven these packages highly stable and reliable.

The Honeywell paper describes its process technology for fabricating multilayer copper-polyimide structures using thin-film approaches. Ronald J. Jensen, John P. Cummings, and Harafdhara Vora, the paper's authors, note that required electrical characteristics such as small propagation delays, minimal signal cross-talk, low loss lines, and high-characteristic impedance impose conflicting demands on conductor and dielectric dimensions.

In general, say the authors, optimal electrical characteristics are achieved by using a high-conductivity material patterned with a large thickness/line-width aspect ratio, a line spacing as large as I/O limits allow, and relatively thick layers (more than 10 μm) of a low-dielectric-constant material. The thin-film copper-polyimide material can satisfy all these requirements.

Honeywell's fabrication of multilayer copper-polyimide structures on ceramic substrates involves a repetitive sequence of conductor and dielectric deposition and patterning processes. CrCuCr conductor layers are deposited by sputtering and patterned by wet etching or ion milling. Polyimide layers are deposited by multiple-spin coating and patterned by reactive ion etching. The authors focus on recent work on the characterization of the spin application and reactive ion etching of polyimide. They also describe multilayer test structures fabricated to demonstrate the feasibility of the process.

A completely different use for polyimide is described in a paper on a small plastic IC package for DIP soldering, by Shigeru Sasaki and three other authors from the Production Engineering Research Laboratory of Hitachi Ltd., Tokyo. They point out that in soldering DIPs, a process where a printed-circuit board is dipped into molten solder, plastic IC packages are subject to thermal-shock stresses, which drastically shorten package life.



1. Flipped out. In this experimental flip-chip package with a silicon carbide substrate designed by Mitsubishi Electric Corp., the substrate's temperature coefficient of expansion matches that of silicon, eliminating any thermal mismatch.

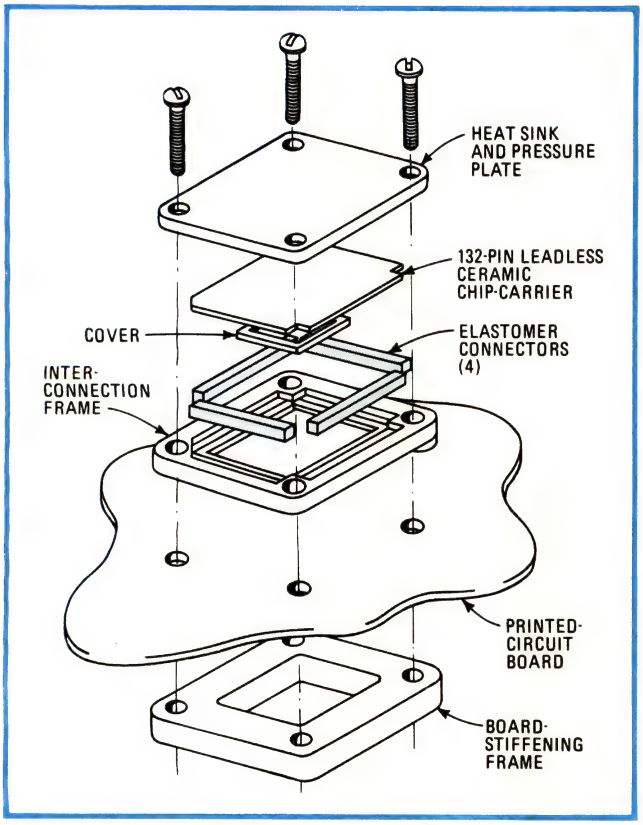
The failure originates in the separation of the boundary surface between a silicon chip and a molded resin and in the formation of cracks in the PSG (phosphor silicate glass) layer that covers the IC chips. These cracks occur mainly because of concentration of stress on the surface of the glass, on which a silica grain used as a filler contained in the resin touches and scratches the glass during DIP soldering. Moisture passes through the cracks and corrodes the circuit patterns on the chip.

Protective layers

In order to solve this problem, the Hitachi group developed a new plastic packaging structure. This new package has a double-stratum structure, which consists of PIQ (polyimide isoindoroquanzolinedione) and PSG for passivation layers. The elastic layer of PIQ is used as a protector of the PSG, which is hard and very dense but fragile. In this structure, the PIQ layer prevents separation of the boundary surfaces and prevents the PSG layer from cracking. In addition, the PSG layer keeps water away from the surface of the semiconductor chip. According to the authors, the new structure, called double passivation, extends the life of this kind of package by a factor of 10.

Another material-oriented paper, by David L. Timmins of Tektronix Inc., Beaverton, Ore., discusses an experimental solderless system for connecting a 132-pad leadless ceramic chip-carrier to a standard epoxy-glass printed-circuit board. This system consists of a ceramic leadless carrier with I/O pads on 25-mil centers, four elastomeric conductive elements, and a molded-plastic frame for positioning the carrier and the elastomeric elements to the board's pads.

Thermal-expansion mismatch ruled out direct soldering of this carrier to a pc board. Leaded chip-carriers,

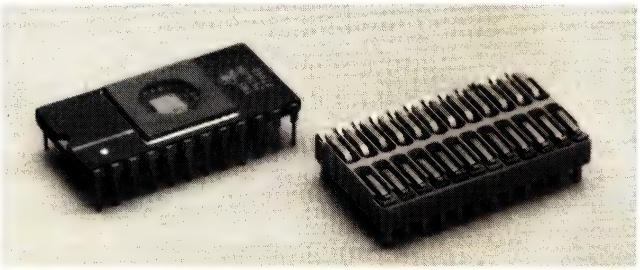


2. Compression contact. At the heart of the components and construction of an elastomeric interconnection system designed by Tektronix are four fine-line elastomeric elements. The entire system is clamped to the printed-circuit board.

another possibility, presented handling problems, and no socket existed for a carrier of this type, so Tektronix had to come up with an original design.

The interconnection selected was a proprietary elastomeric type with photo-patterned metal conductors 3 mils wide on 6-mil centers. A suitable frame for aligning the elastomeric elements to the carrier and circuit-board metalization was designed. The complete package-interconnection system (Fig. 2) consists of a heat sink and pressure plate, chip-carrier, elastomeric connectors, interconnection frame, and board-stiffening frame.

To ensure a good thermal interface between the chip-carrier and heat sink and reliable contact between the elastomeric elements and the pc board and chip-carrier pads, a force of 60 pounds must be applied through the mounting screws. Without the stiffener being used, this force would cause severe bowing of the pc board and could open the signal path from the board to the chip-carrier.



3. Mechanical memory. The DIP socket from Raychem has contacts made of a special alloy that, deformed at low temperatures, will return to its original shape when warmed. This results in a connector with both zero-insertion and high retention forces.

Textronix made time-domain reflectometry measurements on a leadless chip-carrier in the elastomeric package and a socketed 132-pin-grid array. With the elastomeric interconnection, the inductive and capacitive reactance aberrations occur in a much shorter time than in the TDR of the PGA package.

Elastomeric advantages

The author notes that the PGA is an off-the-shelf component, but the elastomeric-interconnected chip-carrier takes up less space, has a lower thermal resistance, and is handled and tested more easily. In addition, it appears that the elastomeric method can easily be extended to even higher pin counts.

Perhaps the most unusual paper to be given at the ECC is one by Regis Flot, Hal Kent, and Tom McGaffigan of Raychem Corp., Menlo Park, Calif., on shape-memory-effect alloys as an interconnection technology. When a shape-memory alloy is deformed at a temperature below its transformation point (a point where a crystal structure change occurs), it will return to its original shape when the temperature is raised. These alloys are based on a nickel-titanium alloy called Tinel.

When an interconnection manufactured from Tinel alloy is cooled below its phase-transformation temperature (–70°C for most connectors), it becomes easily deformed. Once deformed, it will remain so, providing its temperature is kept below the phase-transformation point, even if the original applied stress is removed.

When the temperature rises above the transformation point, the force developed is very high, producing a significant amount of work for a limited volume of material. In effect, the Tinel acts as a transducer, converting heat energy into mechanical energy.

For connectors, a shape-memory alloy offers:

- Zero-insertion/-extraction force when the alloy is cooled and deformed.
- Very high retention force, since it develops high output upon recovery, providing a highly reliable gas-tight connection.
- High contact density and low-profile geometry.

Raychem has made both DIP and PGA sockets using Tinel actuator-contacts. The DIP socket that is shown in Fig. 3 has 24 separate shape-memory-alloy contacts. This design is particularly suitable for socketing DIPs that must sustain severe environments, yet must be removed many times. It can be mated and demated over 1,000 times without causing any electrical or mechanical degradation.

In the PGA socket, a single Tinel actuator simultaneously mates or demates all contacts. A special tool, which must be chilled below the transformation temperature of the alloy, is needed for demating and mating of package to connector.

In the very-high-pin domain, Raychem has designed a ZIF connector using Tinel alloy actuation but with a tuning-fork-type contact, aimed at interconnection of multichip substrates and wafer-scale integration. ☐

Flexible test systems cut costs and hike production-line turnarounds

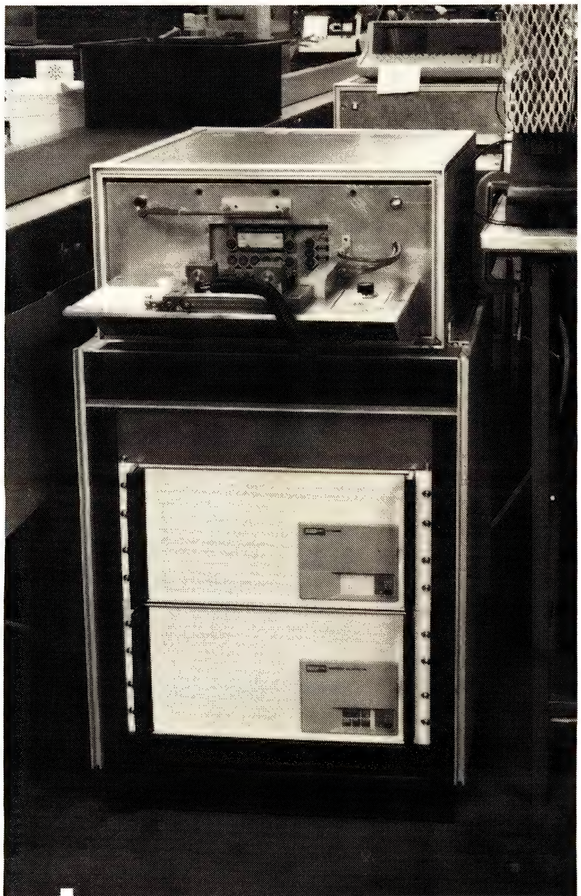
Standard hardware with custom software eases testing of new designs and product revisions

by Joseph Bach and Robert Nickels, *Lake Center Industries, Winona, Minn.*, and
Robert O'Brien, *John Fluke Mfg. Co., Everett, Wash.*

☐ Today's automobiles and kitchen appliances use complex electronic circuits, so the companies that manufacture these high-volume subassemblies need automated test lines to cope with frequent model changes their customers demand. The traditional method of building functional test stations dedicated to a single product is therefore being superceded by flexible software-based systems that drastically reduce turnaround times for product changes, yet do not require that technicians be retrained for each new testing system.

Lake Center Industries, a manufacturer of hundreds of thousands of electronic subassemblies for the auto and consumer-goods market, decided to develop a Universal Test Station that could be reprogrammed to test a wide variety of products. The system performs such tasks as testing incoming components and functional testing both of subassemblies and of the final product. (See "The Universal Test Station in action," p. 139.) To ensure that products perform properly when delivered to customers, much emphasis has been placed on functional testing.

1. Self-contained. The portable test station that Lake Center designed includes a John Fluke 2400A intelligent measurement-and-control system, test on/off switches, and a mechanical test fixture used to handle board checkout.



Until a year ago, almost all functional test systems were designed in house from the ground up, using analog components, digital logic, and microprocessors programmed in assembly languages. These test systems were straightforward, but the building, debugging, documenting, and service needed to make them and keep them operational was very time-consuming. Each new product called for a completely new test system, so all test systems were unique.

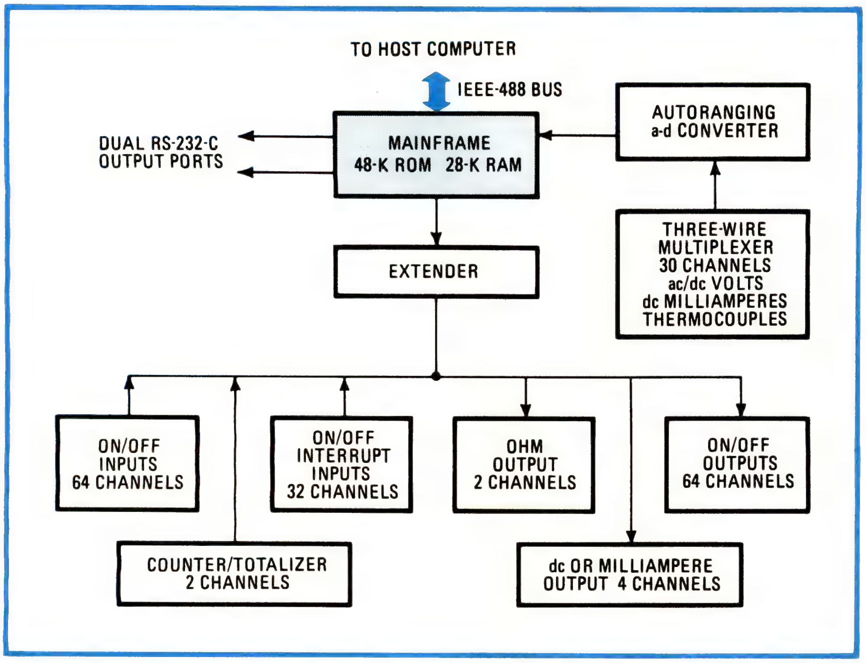
One goal of Lake Center's project was to put 90% of the instrumentation needed for functional testing into one portable test station that could be reprogrammed for a wide variety of tests. Many tradeoffs involving precision, speed, configurations, and computer languages were necessary. For one thing, the new system was meant for use by relatively unskilled technicians. Both hardware and software had to be maintainable, a requirement that imposed certain limitations, particularily on the choice of a programming language.

Had software capabilities been the chief concern, the Forth programming language would probably have been chosen, for it is very powerful in the hands of experienced software engineers. However, Forth would have demanded long hours in training technicians to understand and write test programs, and it would have been difficult for neophyte programmers to update and maintain programs.

The software was designed to be as user-friendly and self-documenting as possible. Processing power was sacrificed for programs that would be easy to write and understand.

Evaluating the available instrumentation and computers took nine months. Many manufacturers and many products were considered, ranging from rack-and-stack IEEE-488-bus systems to multiprogrammers with dedicated computers.

Several options were particularly interesting. An IEEE-488-bus system that relies on the host computer's intelligence can benefit from an almost unlimited selection of bus-compatible instruments. The disadvantage is the possibility that the system might be especially complex, thanks to its complicated programming and diversity of equipment. To


TO HOST COMPUTER
IEEE-488 BUS
DUAL RS-232-C OUTPUT PORTS
MAINFRAME 48-K ROM 28-K RAM
AUTORANGING a-d CONVERTER
EXTENDER
THREE-WIRE MULTIPLEXER 30 CHANNELS ac/dc VOLTS dc MILLIAMPERES THERMOCOUPLES
ON/OFF INPUTS 64 CHANNELS
ON/OFF INTERRUPT INPUTS 32 CHANNELS
OHM OUTPUT 2 CHANNELS
ON/OFF OUTPUTS 64 CHANNELS
COUNTER/TOTALIZER 2 CHANNELS
dc OR MILLIAMPERE OUTPUT 4 CHANNELS

2. Flexible. The 2400A's firmware manages communications with the input/output cards in a background mode, thus simplifying the program's task. With interrupt drive routines, a single station can run multiple tests. The test-station firmware runs a high-level language and handles all I/O timing and communications functions.

achieve optimal results, programming an IEEE-488 bus system with a controller and three or four slave instruments—each with some intelligence and different mnemonic command sets—demands an experienced software professional.

Finally, an IEEE-488 system that puts the intelligence in one input/output device was chosen. A desktop computer develops the test programs, but once the system is up and running, the computer can be unplugged and used elsewhere. Programming has been made less complex and more structured, since the test application software does not have to manage I/O operations, now performed by the intelligent front end's operating system. Although the system's performance has been limited, what can be done is very well defined and streamlined.

Test networks

Another important consideration was the intent to link test equipment in networks at some time in the future. In such networks, it will be desirable to have intelligence distributed at each node, so that the central computer will be able to download programs and collect data while each node operates autonomously.

Various trade-offs are commonly encountered when evaluating instrumentation of this type. Since most high-speed measurement systems gain throughput at the expense of precision, the importance of both speed and precision were carefully considered. In the end, it was determined that 16-bit precision was required and that the consequences of a slower system were easier to compensate for than a lack of precision would be.

For the intelligent measurement-and-control instrument, the Fluke 2400A was chosen; for the computer, the choice fell on the Hewlett-Packard HP-85, a complete computer system, with a video display, cassette storage system, and a printer all in one package. Such an all-in-one package may be used on the factory floor, in the office, and at home when deadlines approach.

Communications between the HP-85 and the 2400A over the IEEE-488 bus are straightforward. The two machines can be brought up and running on a fundamental level very quickly; all that is needed is an HP-85 program with about 10 lines of Basic code added. The designers could have chosen a more powerful computer, of course, but cost was a major concern, and the HP-85 met the needs of the application.

The main difference between the Fluke 2400A and other I/O devices is its local intelligence, the chief reason for the unit's selection. Its operating firmware, contained in 48-K of read-only memory, handles all I/O timing and communications. The language of the 2400A resembles a cross between Basic and Pascal, is structured, and has a reputation for ease of maintenance.

Error handling is a major plus for the 2400A. Like most computers, it sends numerical error codes for hardware malfunctions and software syntax errors. In addition, it checks the application program for fatal programming errors; for example, it will detect a Call command referencing a nonexistent subroutine or a variable name that was mislabeled during input.

In Basic, these errors can go unnoticed for quite a long time, especially if the program rarely branches to the location of the error. When it does surface, the program would merely stop, and there would be no error code to help find the problem. In contrast, the 2400A will not run a program with such errors but will generate an error code—for instance, "call to nonexistent procedure."

Mixing different manufacturers' products in the same system was not a concern, since they talk over the standard IEEE-488 bus. When actually performing tests, the station was designed to operate independently of the HP-85. For inputs and for outputs, the system has most of what it needs. Precision is assured by the 2400A's 16-bit analog-to-digital converter; time, however, was sacrificed. At the very best, the system takes 33 milliseconds to read an analog voltage.

Test station hardware

Mounted on wheels, Lake Center's test station (Fig. 1) contains the Fluke instrumentation, brackets for mounting the mechanical fixtures, a console for mounting all operator controls, and space behind the operations console for mounting custom boards. Figure 2 shows a block diagram of the test station. The autoranging a-d converter can measure anything from 1 to 100 volts with 0.01% accuracy. The 2400A's firmware automatically manages all communications with the I/O cards and gives users a

The Universal Test Station in action

Simulation is the best way of testing a complicated piece of equipment with a heavy electronics content, using a stimulus/response transfer function identical to that of the final product. An example is the most recent sophisticated climate controls for the interiors of automobiles.

Typically, these controls incorporate a microcomputer that monitors various analog sensors through a built-in analog-to-digital converter. These inputs may be temperature-sensing thermistors or voltages used to position the motor-driven actuators that control the car's comfort level. Special duty-cycle circuits drive the blower fan to produce a variable airflow, and a digital display and keyswitch array permit the driver to select various modes and temperature settings.

A software program that can fully test and exercise the functioning of a complex controller uses the Universal Test Station with little external hardware. Programmable resistance outputs simulate varying thermistor inputs, and analog voltage outputs provide feedback for the climate control's microcomputer, just as motor-driven actuators do in an actual automobile on the road. Multiple interrupt-based processing permits the test system to observe events that occur almost simultaneously and to emulate the in-car response to quite a variety of climate-control situations.

Under program control, status-control output lines select loads and place the control unit into specific modes by means of air-solenoid-powered mechanical button pushers that depress the touch-sensitive switch panel. The test system electronically senses display information by using phototransistors or image sensors, interfaced through external conditioning hardware to status-input channels. Even the blower fan's duty cycle can be measured accurately with the counter-totalizer input to the tester.

With this hardware-software combination, the climate-control system can accurately and fully evalute and test the device, with results analyzed statistically. A test sequence of more than 50 measurements runs in less than three minutes. Thanks to the mechanical button pushers, such a sequence requires an operator only to load and unload the devices under test.

At start-up, in order to permit engineering and quality-assurance personnel to observe and evaluate the test system and the product, the actual measurement values may be printed on the HP-85 computer. Often, if the computerized test station's reports are analyzed, start-up process and component problems can be detected early.

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high-level programming language.

When customized test electronics, like a power supply or a 20-kilohertz a-d converter, is called for, it would usually be turned on and off and read by one of the 2400A's cards, so that the whole test was run by a single application program. Often, a test will not need all the I/O or processing power of one test station. Interrupt-driven subroutines let such a station run multiple tests, and as a result, a standard 100-pin connector and cable has been set up to run the 2400A I/O lines to extender stations. These extenders are identical to a fully loaded station except that they do not have the 2400A.

Designing tests for new products is simplified, since the technicians know exactly what control outputs and measurement inputs are available and the pins on which they are located. This minimizes new hardware design and simplifies documentation.

Application software

The key to making the computer a powerful test tool is choosing a system that is friendly enough to be used by relatively inexperienced technicians. The thermistor test program in Fig. 3 illustrates this point.

Thermistors are used to sense the temperature inside automobiles. They are less easy to test than they might seem to be. Putting the units in a fixture next to a reference thermistor and comparing the two temperatures is the basic testing procedure. The main problem is determining when the thermistor under test has stabilized.

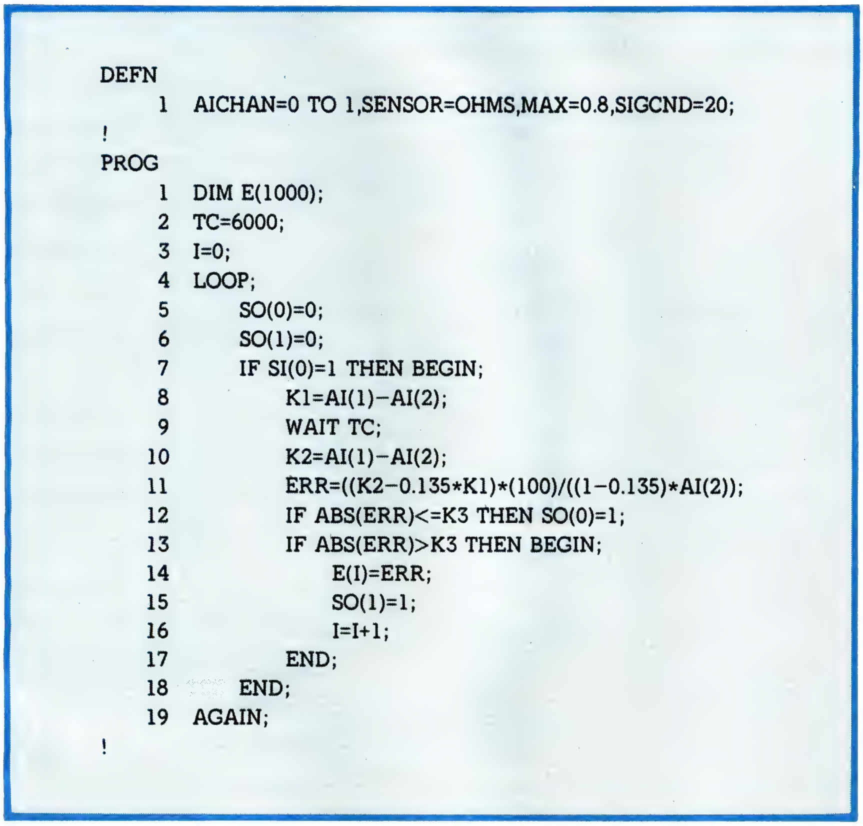
Former methods required operators to use their own judgment by watching a gauge. The test station created in this project can compute the thermistor's stabilized value, thus shortening test times and eliminating the possibility of human error. In the program in Fig. 3, both thermistors are measured twice, with a time delay that equals two thermistor time constants between readings. The thermistor's time constant is a known value, so the application program can compute the settled reading without waiting for it to stabilize. On line 10 of the program, the settled reading and the projected percentage error are computed and stored in the variable called ERR.

The thermistor's error tolerance—a constant that can be changed at any time even if a program is running in the test station—is stored in variable location K_3. The host computer simply prints a statement like "K3 = 3 !" at its IEEE-488 output, and the value of error-tolerance variable K_3 then changes to 3. This capability is used during start-up and also for debugging in the event of high failure rates.

Pass/fail indicator lights are turned on by status output channels, which are open-collector TTL switches. The test results are stored in array variable E(I). This valuable information can be sent to a printer directly though the test station's RS-232-C port or collected by the host computer. The program in Fig. 3 uses English-like commands and is easy to read and understand.

Test programs are typically developed in the immediate mode. Separate commands are sent one at a time from the HP-85 to the 2400A and the results observed. When the various elements of a testing sequence have been performed separately, the commands are strung together and loaded into the 2400A. The HP-85 becomes inessential and is only needed for diagnosing problems, making changes, and collecting statistics. The cost-effectiveness of the test station's independence is obvious: only one HP-85 is needed to handle a number of 2400A test stations.

Structuring and modularizing programs is the key to



```
DEFN
        1   AICHAN=0 TO 1,SENSOR=OHMS,MAX=0.8,SIGCND=20;
!
PROG
        1   DIM E(1000);
        2   TC=6000;
        3   I=0;
        4   LOOP;
        5       SO(0)=0;
        6       SO(1)=0;
        7       IF SI(0)=1 THEN BEGIN;
        8           K1=AI(1)-AI(2);
        9           WAIT TC;
       10           K2=AI(1)-AI(2);
       11           ERR=((K2-0.135*K1)*(100)/((1-0.135)*AI(2));
       12           IF ABS(ERR)<=K3 THEN SO(0)=1;
       13           IF ABS(ERR)>K3 THEN BEGIN;
       14               E(I)=ERR;
       15               SO(1)=1;
       16               I=I+1;
       17           END;
       18       END;
       19   AGAIN;
!
```

3. Test program. In the program listed, two thermistors are measured twice, with a time delay equal to two thermistor time constants. The settled reading is computed and stored in the variable called ERR.

maintaining software. The 2400A language enforces discipline in these areas: it does not contain Go To statements, which limit its flexibility, and avoids the jumbled mess many novice programmers get themselves into with Basic. Modularity is achieved through the use of subroutines entered either by a Call statement or contact closure on an external interrupt line. It is common to use 15 or 20 subroutines of 10 or 20 lines each and as few as 20 lines in the main body of the program.

Collecting data can potentially complicate programs, since it can involve communication over the IEEE-488 bus between the test station and the host computer. Using variables in the 2400A to store the readings taken during a test helps avoid most of this problem. At the test's end, a 2400A command can cause a service request to be sent to the HP-85, which can then collect the data in a background mode without interrupting the next test.

IN-HOUSE VERSUS UNIVERSAL TEST STATIONS

	Test stations designed in house	Universal test stations
Electronics: capital cost	$ 15,000	$ 60,000*
Mechanical fixture: capital cost	$ 18,000	$ 18,000
Engineering: cost at $5,000 per man-month	$ 25,000	$ 45,000
Drafting, assembly, debugging, and documentation: cost at $2,000 per man-month	$ 90,000	$ 20,000
Total cost	$145,000	$140,000

*Recoverable at the end of the product life cycle, since the universal test station could be reused for another product.

For example, the HP-85 Basic statement might be "Output 702; Send A !" This would make the 2400A pause, put the value of the 2400A software variable A into an IEEE-488-bus output buffer, and then continue where the intelligent measurement-and-control system left off. The HP-85 can then use an input statement to collect variable A without further interrupting the 2400A's test program. In all probability, the test program has already established the needed variable in order to check the test parameters against stored limits. As a result, the whole data-collection function can be implemented in HP-85 Basic, without any need to add code in the 2400A.

A software-based test system also promotes easy modification of pass/fail tolerances, since they are stored in the 2400A as variables. This has proved very useful during startups, since it makes the system flexible enough to adapt tests to what is achievable and to make special production runs with tighter-than-standard test tolerances. In the past, this would have required either a hardware change in a tester or special instructions to the production workers, both choices fraught with difficulty.

Dramatic savings

The new testing strategy's most important result has been dramatically to reduce the flow times and manpower needed to get new products into production. As the comparison in the table shows, total project costs for universal test stations and dedicated ones are about the same. Capital costs have gone up and man hours have gone down. However, since the universal test station is reusable, while in-house dedicated testers are not, the universal approach comes out ahead financially.

What the cost comparisons do not show are the savings in repair costs, the flexibility needed to make changes easily, and the improved quality of test methods. Moreover, reduced flow times promote responsiveness to customer needs and the ability to handle new business. It is now practical to build one product on Friday, to convert the line over the weekend, and to build another product on the following Monday. The test software and mechanical fixture can be developed on the same test station. To convert the production line, the test engineer simply loads new software into the old test station, changes fixtures, and is ready to go. An added benefit is the ability of the computer to record test results and test parameters rather than just pass/fail indications. ☐

High-temperature wafer prober predicts yield problems early

A novel semiconductor test head, used just before scribing, puts wafers through high-temperature dynamic testing usually left for final test

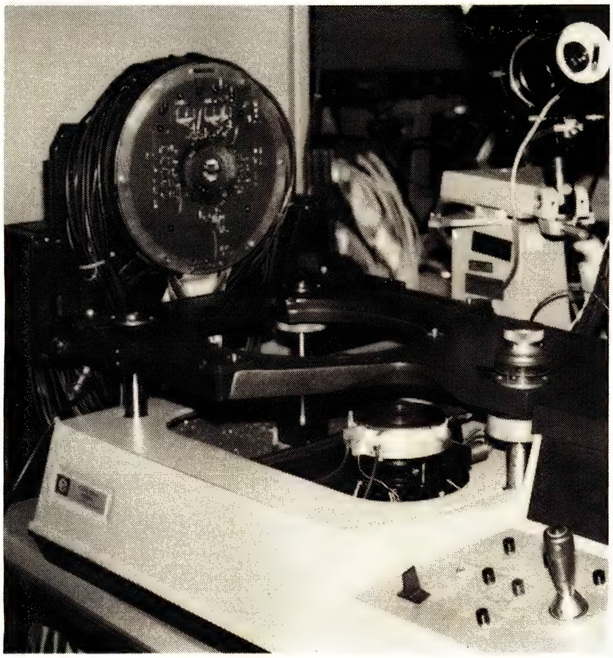
by Douglas A. Buol, *Texas Instruments Inc., Military Products Department, Semiconductor Group, Dallas, Texas*

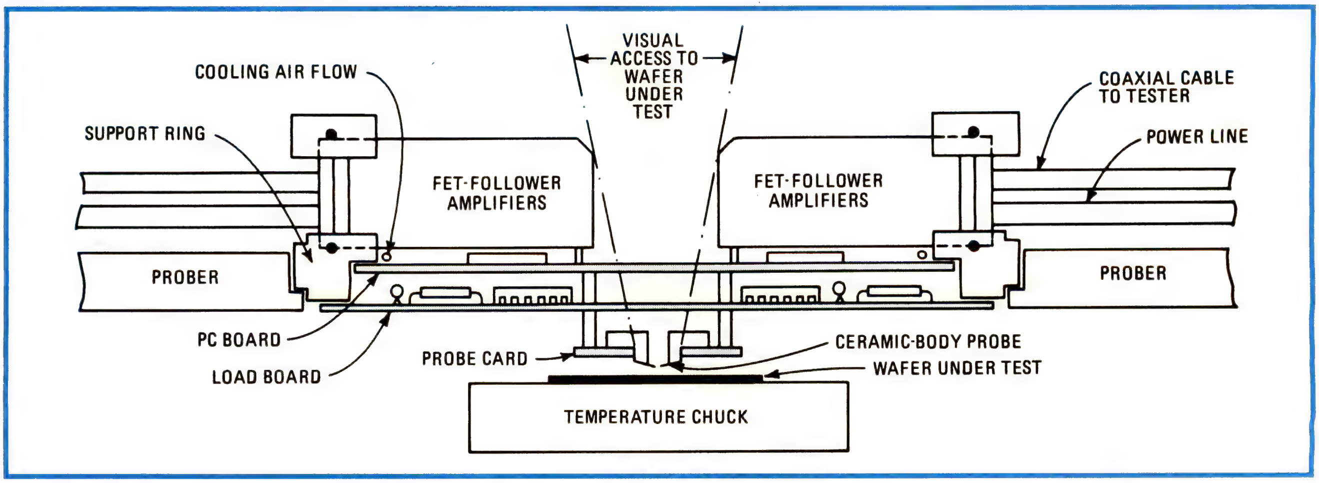
☐ When an excessive number of failures shows up in packaged chips during final testing, the culprit is often subtle process or material shifts that were not picked up during static room-temperature wafer-probing tests. One way to detect these defects before the final test stage is to implement a dynamic high-temperature electrical test during wafer probing before they are scribed into individual chips. A wafer prober designed to operate both at high frequencies and at high temperature can do this.

In a typical case, quad operational-amplifier chips that yielded better than 70% good parts in room-temperature wafer-probing tests began failing at an alarmingly high rate in the final-assembly test. When the next production lot, with even higher room-temperature yields, was subjected to probe testing at 125°C, the wafers showed a yield of merely 3.8%. Those parts that passed, however, provided yields of 99.6% at 125°C and overall yields of 98% at final testing when fully assembled, so there was a great overall savings in assembly costs despite the much lower wafer-level yield. Clearly, 100% testing of such wafers at high temperature is desirable—and economically justified.

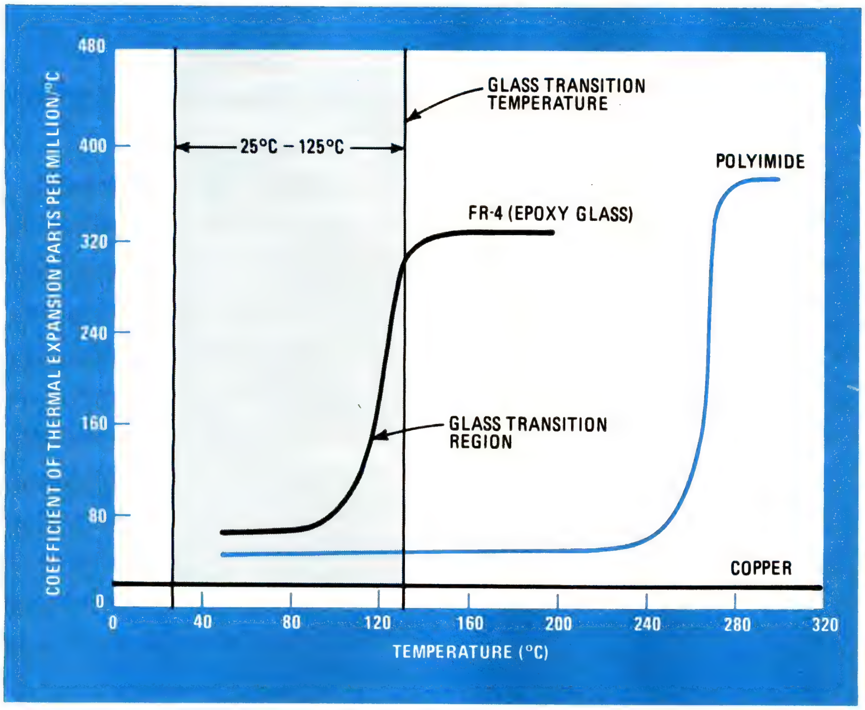
Minimizing costs and unexpectedly low yields at final testing of both linear and digital parts translates into on-time deliveries and competitive prices to the customer. For chip buyers in the hybrid industry, their suppliers' heightened ability to find potentially defective chips at the wafer level can improve incoming-chip quality and reduce costly rework. Short-term economic advantages aside, when high-temperature dynamic-yield problems are revealed during wafer probing, superior failure analysis can rapidly identify and solve the basic problem.

Often the most valuable





1. Triple decker. The high-temperature wafer prober (top) consists of a circular stack of three annular polyimide printed-circuit boards, a support ring, temperature chuck, and temperature test head for changing probes and boards. Each board (bottom) serves a different function.



2. Thermal expansion. At 125°C, FR-4 (flame-resistant G-10 epoxy glass) has more than four times the thermal coefficient of expansion of polyimide. As a probe card made with FR-4 expands and contracts, its probes lose contact with the pads of the wafer under test. For this procedure, therefore, polyimide is the material of choice.

clue to solving the root-cause riddle—visual and electrical comparison of good and bad circuits on the same wafer—vanishes as wafers are diced into chips and packaged in assembly. Should the design need to be changed, it is quicker and less expensive to evaluate a new design when wafer testing includes high-temperature stressing instead of running only the usual package tests.

Hot probing

If high-temperature wafer probing is such a good idea, why has it taken so long to put it to use? The fact is, it has been tried but not successfully. Most multiprobe systems work at controlled room temperatures. But when temperatures are cycled from 25°C to 125°C or beyond, the thermal expansion and contraction of the probes and their supports cause the probes to intermittently lose contact with the die under test or move out of the acceptable test area on the die surface. Such movement can produce faulty test results and even allow operable wafers to be rejected.

Thus the accuracy and repeatability of high-temperature tests are limited by the thermal effects on the probing system's various components. A typical system includes several extremely thin metallic probes mounted on a support, such as a printed-circuit board, and arranged in a pattern to contact the areas on the die to be tested. A special chuck holds and positions a wafer to place each die successively into contact with the probe assembly.

A single probe is about 1 mil in diameter and must accurately contact an area on a die that is in only about 3 to 4 mils on a side. Also, most probes need the angular positioning to be accurate within about ±0.25°. At a relatively constant room temperature, these small dimensions hold quite well for long periods, but wide temperature swings quickly upset them.

Dynamic testing at high temperatures requires a very special probing assembly. One approach, shown in Fig. 1 and in use at Texas Instruments, is a three-tier stack of annular pc boards made of polyimide glass, each with a separate function.

The top board consists of lead-switching components required for testing digital parts. It is not required for testing linear ICs, such as operational amplifiers, where a two-tier test head is used. Spacing it away from the temperature-controlled chuck and forced cooling air keeps its temperature-sensitive components under 35°C, even during 125°C testing.

Circular boards

The middle board contains loads for ac testing of the unit under test and connections for the dc parametric inputs. Both the top and the middle boards are circular in shape, 0.093 inch thick, and securely attached to the support ring every 60° at their outer circumference and to each other at three points near their centers. To keep noise low, all three boards have full ground planes and multiple connections to the support ring, which is connected to the test-system ground.

At the top of the assembly, field-effect-transistor circuits buffer, amplify, and transmit the dynamic waveforms from the die being tested back to the test system. These circuits are arranged concentrically in order to minimize lead length (to less than 2.3 in.) between the test pads on the wafer and the FET amplifier inputs; yet the operator can see the probes in their entirety. The support ring securely holds the FET probes and attached cabling in one rigid assembly, so that the boards under the head are not stressed. Because the assembly is circular, the probes can be rotated for theta adjustment; the operator can use the lift assembly to raise and rotate the test head 90° as one unit for each access to the probe card.

A 3-in.-diameter board, suspended below the middle board and closest to the high-temperature source forms the probe card. Ceramic probes are mounted on this card, whose position and size makes changing the probe card easy. The unit serves as a thermal spacer between the high-temperature surface and the active components on the upper-level boards.

The polyimide solution

Polyimide laminate was chosen for the prober's cards over the more popular G-10 epoxy glass because of polyimide's favorable high-temperature expansion characteristics. As Fig. 2 shows, the coefficient of thermal expansion for FR-4 (flame-resistant G-10) epoxy-glass material rapidly changes in the 80°C-to-130°C range, as it passes through its glass-transition temperature. At 125°C, FR-4 has over four times the coefficient of thermal expansion that polyimide has.

Unlike most common materials, which come in either crystalline solid, liquid, or gas, polymers pass through a glass-like state. Therefore, the epoxies used as binders in FR-4 pc-board laminates do not have fixed melting points but soften over a temperature range centered on a mean value called the glass-transition temperature.

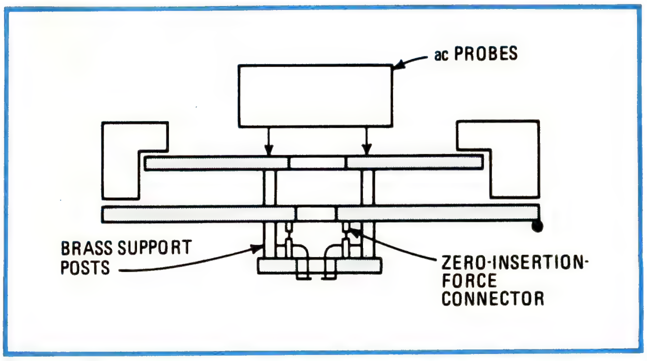
In this region, rapid changes in the coefficient of thermal expansion, and in dielectric constant, density, specific heat, and elastic modulus also occur. The high coefficient of expansion and softening at 125°C of the FR-4 material makes for unacceptable movement of the probe tips during testing: when the probes and probe supports expand and contract, the probe tips move, which in turn can cause the probes to intermittently lose contact with the die under test or to move outside the contact area.

Early attempts to carry out high-temperature dynamic testing with a multiprobe setup using standard FR-4 probe cards with conventional long copper probes produced more than a 1.5-mil translation of the probe tips when the temperature was changed between 25°C and 125°C, frequently creating "probe-into-overcoat" or "probe-off-pad" visual rejects. By contrast, the test head built with polyimide and short ceramic-probe bodies reduced this translation to less than 0.5 mil.

Dynamic testing

In the conventional probing arrangement, digital-die testing on a processed wafer is generally done at 25°C by coupling logic-test signals to the inputs of a die and sensing the output levels' signals to determine proper operation. This is referred to as static, or dc, testing since the output levels are measured after they reach steady-state.

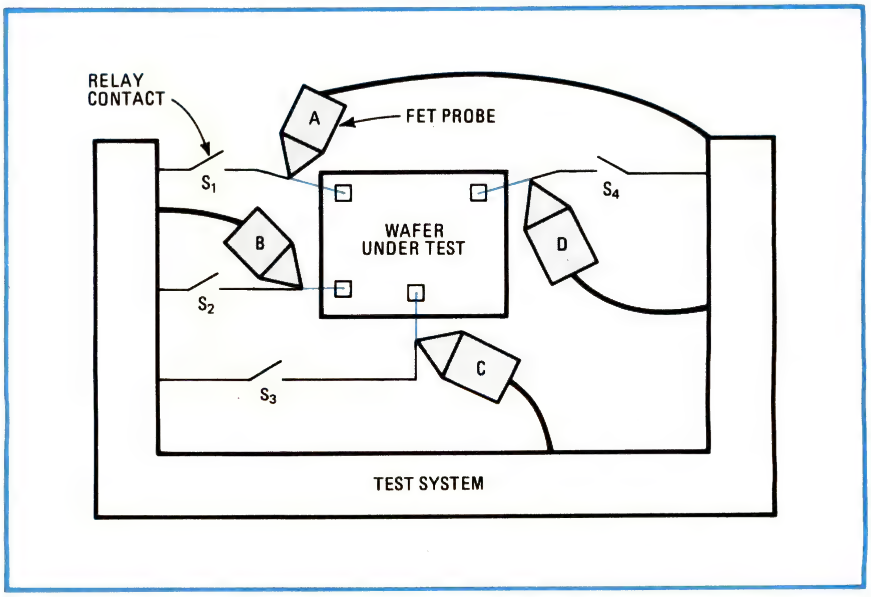
Though static testing is important in predicting whether a device will be operable following assembly and packaging, it does not ensure that a completed chip will pass a final test that simulates operation at normal operating frequencies and switching speeds. Needed are dynamic, or ac, tests to more accurately predict which dice will pass a similar final test after completion. Dynamic testing of digital circuits includes applying high-speed logic signals to the dice while sensing the outputs to measure operating parameters such as propagation delays and switching speeds under load conditions.



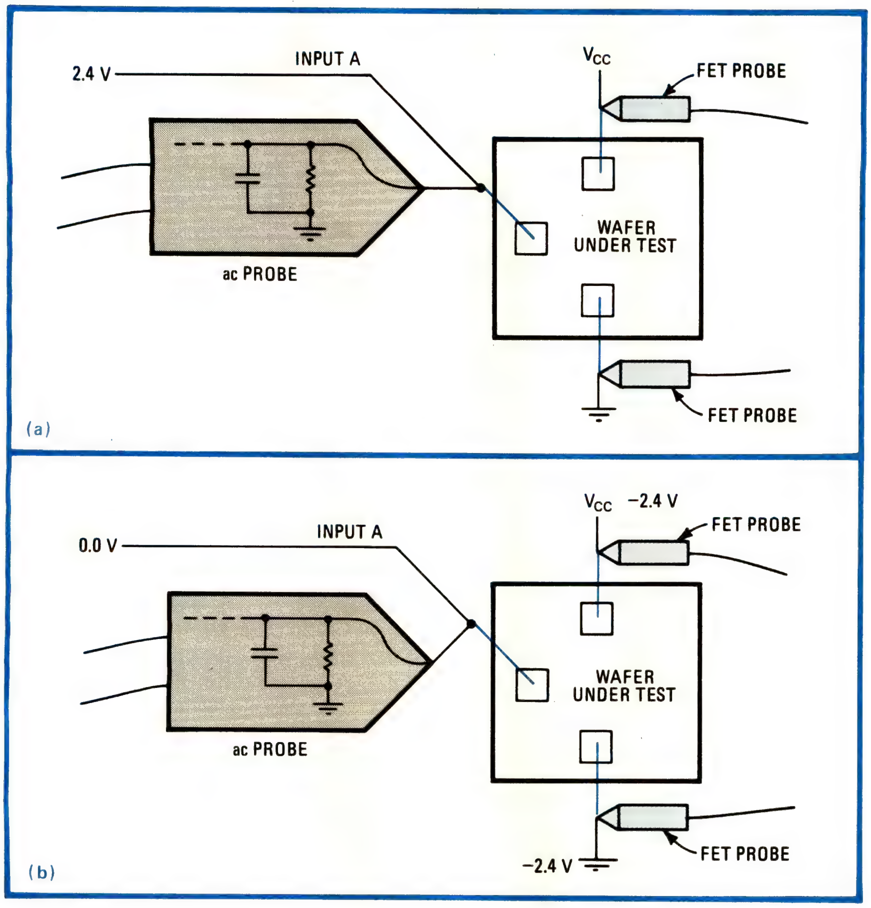
3. Stress reduction. In this high-temperature prober, the 0.093-in.-thick polyimide probe board with short ceramic probes, front support posts, and zero-insertion-force connectors reduce mounting stress. These features prevent board flexure and probe movement.

For high-frequency dynamic testing, the direct-connection paths between the pads on the unit under test and the probe card's FET-sensing inputs have to be as short as possible. Standard edge cards have long leads and are not suitable. If connections are made very near the probe bodies on the standard probe cards at 25°C, however, the ac probes flex the probe card and move probe-tip positions off the pad. On the new prober, a thick probe card mounted on the front has zero-insertion-force pins to reduce mounting stress so that the probe's position does not change from the original setting when the probe assembly is mounted on the dynamic-test head (Fig. 3).

When a single fixture is used for both dc-parametric and ac-dynamic tests, manufacturing throughput im-



4. Combined testing. This configuration can be used for both dc-parametric and ac-dynamic testing. The FET-follower probes are connected as closely as possible to the wafer under test in order to avoid stray capacitance. The followers buffer dynamic signals.



5. Leakage errors. A leakage measurement on input A will be in error because of the input probe's shunting resistance (a). If the input pin is programmed to 0.0 volts and V_{cc} and ground levels are shifted as shown in (b), however, no error current will flow out of or into the FET-follower probe.

proves greatly. But such combined testing is seldom done with conventional probing assemblies—even at the final test. Generally, different test hardware and component handlers must be used for the dc-parametric and ac-dynamic testing, and the material flows serially through the testers.

Should the special multiprobe test fixture be used, however, both types of tests can be done accurately in one combined test assembly (Fig. 4) with one caution: to avoid the extra capacitance and lead length of relays S_1 through S_4 during dynamic testing, all FET-follower probes were designed for direct connection to the pads of the unit under test. Relays S_1 through S_4 are computer-controlled to provide inputting or sensing functions as required for dc testing. FET follower probes, labeled A, B, C, and D in the figure, isolate and buffer dynamic signals back to discriminator circuits for dynamic tests.

During nanoampere and microampere leakage measurements, significant error can be introduced (Fig. 5a) by FET-follower probes having even 1 megohm of input impedance. But arranging the leakage-test bias conditions as in Fig. 5b ensures that both dynamic and static testing may be done accurately on digital parts within the same test fixture.

Accelerating infant mortality

Moving the burn-in step from the board level to the component level to the wafer level has several distinct advantages. Besides cost savings, burn-in at the wafer level may be performed at much higher temperatures, thereby accelerating infant-failure modes.

On wafers picked at random from specific lots, accelerated acceptance testing may be performed, say, at 250°C for 15 minutes in order to identify parametric shifts on selected chips containing test transistors. For example, for failure modes that require 1.0 electronvolt of activation energy, 15 min at 250°C is equivalent to operating the chip for about 265 hours at 125°C or for many millions of hours at 25°C, depending on the failure modes' activation energy. Class B or Class S chip-reliability levels, which require burn-in for 160 or 240 h at 125°C, respectively, may be approximated by such accelerated temperature techniques. The equivalent values are based on the thermodynamics of chemical reactions, called the Arrhenius Equation, in which the rate of a chemical reaction doubles for every 10°C increase in temperature.

The advantages gained from an accelerated test—savings in time, facilities, and personnel—must be tempered by the possible introduction of extraneous failure modes from excessive temperature. Each failure mode needs careful in-depth analysis to see how it is affected by temperature. Also, circuits may need adjustment of biases and other voltages to prevent incidental damage and retain operational ability.

With such testing, it would be possible to get predicted life distribution in hours, rather than in years, of operation. Acceptance for selected key stability factors can be quickly obtained, low-activation-energy failure modes (responsible for mortalities) can be rapidly established, and checks can be swiftly made on device lots to detect process drift or material contamination. ☐

Wideband local nets enter the computer arena

A proposed standard for wideband local networks joins three competing commercial products

by W. E. Burr and R. J. Carpenter, *National Bureau of Standards, Washington, D. C.*

☐ Local networks for personal computers have received a good deal of attention, but few people know much about the work now under way to standardize local-net protocols and connections for mainframes and supercomputers. Several manufacturers sell wideband networks that are now quite expensive—from $20,000 to $50,000 a connection—but the timely introduction of a standard will encourage the development of custom large-scale integrated parts, provide for alternate network suppliers, and promote competition in the marketplace. It will therefore tend to drive prices down and also extend the benefits of wideband broadcast networks to an ever-larger base of users.

In the U. S., three such networks with data-transfer rates of 50 megabits a second or more are now available commercially. Hyperchannel, a product of Network Systems Corp., Brooklyn Park, Minn., offers adapters to connect it to the input/output interfaces of about 20 common but diverse supercomputers, mainframes, minicomputers, and operating systems, from more than a dozen manufacturers.

The Loosely Coupled Network (LCN), from Control Data Corp., in Minneapolis, is the I/O interface on the Cyber 205 supercomputer. Adapters are also offered for the I/O channel (Federal Information Processing Standard 60) and the Unibus.

The Computer Interconnect (CI), Digital Equipment Corp.'s high-bandwidth local network, connects up with the company's VAX computers. It is the interconnection for the DEC "cluster" concept—the Maynard, Mass., company's new thrust in large and high-availability multicomputer systems.

Finally, a fourth wideband local network has been drafted by American National Standards Committee X3T9.5. This Local Distributed Data Interface (LDDI) is in fact electrically identical to the LCN, but its protocols are really more like those of Hyperchannel and CI.

All four are back-end networks: they connect computers to secondary storage, such as magnetic disks and tapes, as well as to nearby computers. They thus form loosely coupled multiprocessor systems—or at any rate, systems that are loosely coupled when compared with those designed with shared main-memory multiprocessors. Even so, they are much more closely coupled than open systems, which use general-purpose, comparatively slow telecommunications protocols to join widely separated computer systems.

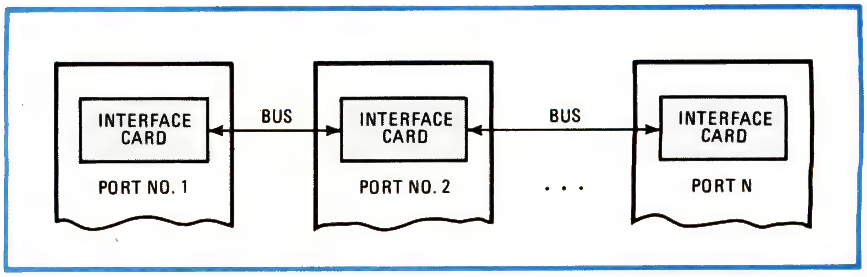
The closeness of the coupling that any network provides has two performance dimensions: latency (the host-to-host time delay induced by the network) and bandwidth. In principle, wideband connections are possible at any distance, but the speed of light makes latency increase with distance. Latency absolutely limits closeness of coupling for multiprocessor systems that use long-distance telecommunications networks.

A few big computers

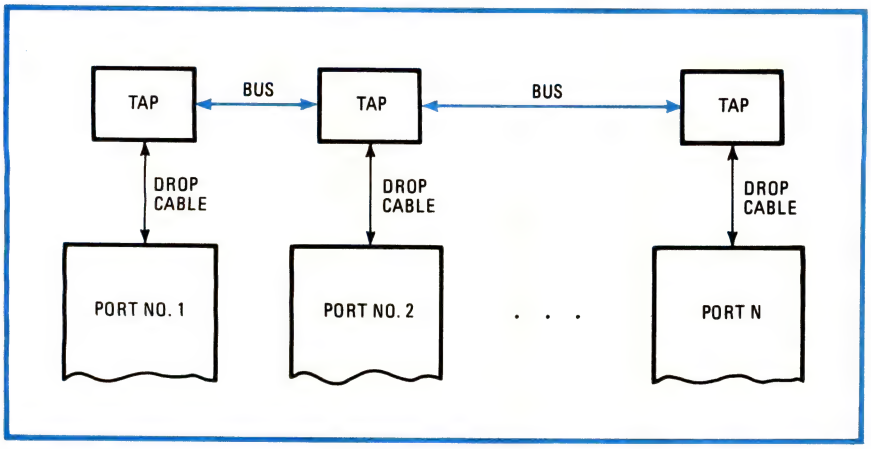
All four of the networks can connect at least 16 comparatively large computers and storage devices over distances of less than about 1 kilometer. All of them reduce or eliminate collisions by using some version of the carrier-sense multiple-access (listen-before-talk) protocol for network arbitration.

By contrast, lower-bandwidth networks that are oriented to terminals or work stations can be used to couple small computers and peripheral servers with comparable closeness but over somewhat greater distances. The wideband broadcast networks described in this article are used primarily with large minicomputers, mainframes, and supercomputers.

A broadcast network is any network where one port transmits a message and, after a propagation delay, all



1. Hyperchannel topology. The Hyperchannel uses a bus topology; the cable runs through an interface card that is part of the host system's port. If any port is removed from the system, the whole network comes down until the cables are reconnected.



2. Looks like the LCN. The Local Distributed Data Interface (LDDI) and the Loosely Coupled Network (LCN) use identical topologies. A port may be disconnected while other network participants continue to transfer data. End-to-end transmission runs are usually limited to 1 kilometer.

other ports on the network receive the message without intervening storage or switching. Broadcast networks may have one channel or two (send and receive) and a bus, star, or tree topology.

Switched networks and rings are two other, fundamentally different, kinds of local nets. In local networks, the propagation delays of switched networks are quite small compared with typical packet-transmission times. Hence, the number of bits on the fly divided by the packet size becomes an index to the "localness" of the network. At 50 Mb/s, with 1 km of cable, there will be some 250 bits on the fly, and a typical message in these networks will have from 10^3 to 10^5 bits. Viewed in this way, wideband nets, too, are local networks because packet sizes are typically rather large despite the significant propagation delays.

Match to OSI model

Although the seven-layer Open Systems Interconnection model is commonly used to describe computer communications, of the four networks discussed only the LDDI was originally conceived in those terms. Wideband networks are chiefly concerned with the lowest three layers—the physical, data-link, and network layers—because only they are visible to the actual communications medium. Moreover, in isolated local broadcast networks, it is sometimes hard to distinguish between the network layer and the one above it, the transport layer.

The physical, data-link, and network layers each have a protocol that communicates with its analogous layer at the other network ports by means of the interface between the layer and the one that is just below it and the services it provides. At the physical layer, communication with peers takes place through a shared medium for interconnection.

It is hard to use the OSI model to describe broadcast networks because it addresses switched networks—a number of switching nodes connected by point-to-point connections—rather than broadcast ones. The essential concern of broadcast networks is arbitrating the shared medium of interconnection, and arbitration is not considered in the text of the OSI model.

The model tabulates functions that may be performed at each layer, but in the lowest three layers, only two functions are assigned uniquely. Transmission error detection is assigned exclusively to the data-link layer, while routing is solely the domain of the network layer. Any partitioning of a system into the lowest three OSI layers must rely upon these two points.

The medium for interconnection physically connects the network ports. In broadcast networks, unlike switched ones, a single medium interconnects all ports. All protocols operating on data that is not checked by the message frame-check sequence (FCS) are properly ascribed to a physical-layer protocol, which includes the encoding and decoding of data bits to signals suitable for transmission. In most carrier-sense multiple-access (CSMA) networks—where the medium's arbitration depends only on its analog state and not on the contents of any data transmitted—the arbitration of the interconnection medium is a physical-layer protocol.

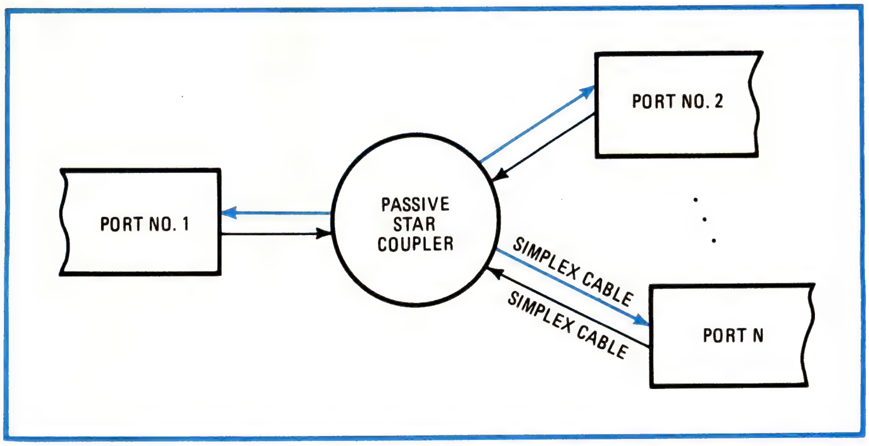
Essentially, the data-link layer's business is to check messages for transmission errors—a function performed by the FCS in the wideband networks under discussion. The algorithm divides the message by a carefully chosen polynomial and uses the remainder as the frame check.

In principle, error recovery could be performed with a forward error-correcting code and would thus be a data-link-layer function. In practice, local networks never use this technique, because error rates are so low that it is more effective to retransmit the occasional damaged message. Address recognition at stations—not a concern in switched networks and not mentioned in the OSI model—must occur at the data-link layer or above, since the FCS always checks addresses. If the message length is delimited by a length field checked by an FCS, end-of-message framing is also a function of the data-link layer, for it is the lowest one that operates on data whose correctness has been checked.

Smarts at the top

All communications-related intelligence is generally assigned to the network layer. (This is permitted, though not required, by the OSI model.) The network layer's essential business is routing. Since a single broadcast interconnection medium needs no special routing function, some people argue that in broadcast networks, the network layer is null. This contention may be reasonable for terminals and for work stations, but all these high-performance broadcast networks feature redundant parallel media to improve performance and reliability and automatically route messages around bad paths. It fol-

3. New star? The Computer Interconnect (CI) is a star topology. At 70 megabits a second, its data-transfer capabilities are the best of the four systems, but the transmission distance from the star coupler to any port is currently limited to 45 meters.



lows that there is indeed routing and a network layer.

It is also convenient to ascribe to the network layer other processes requiring intelligence, such as acknowledgment of messages and retransmission of damaged frames. At present, the standards community is very much concerned with an "internet" protocol, which fits between the transport and network layers and connects heterogeneous networks. An internet protocol's existence is not even hinted at in the OSI model, yet many observers think that such a protocol includes the whole network layer.

Just above the network layer, the transport layer is end to end, and its services may operate over several concatenated but dissimilar networks. The transport layer can provide such end-to-end functions as lost, duplicate, or out-of-sequence message detection. Since local broadcast networks provide a complete end-to-end service, they tend to make no clean distinction between network and transport services. Although these networks frequently do provide services that are perhaps on the transport level, no distinction between the network and transport layers is needed.

Cable interface

Two of the four networks, CI and Hyperchannel, use baseband signaling, Manchester coding (a self-clocking code that uses as many as two signal transitions to send one data bit), and a 50-ohm coaxial cable. The hardware implementation is comparatively cheap, but baseband transmission uses all the medium's available bandwidth for interconnection.

The LCN and LDDI use an identical interface: broadband signaling on a 75-Ω coaxial cable—a scheme that employs 180° phase reversal change on zero modulation of a 150-megahertz carrier, accompanied by a 50-MHz clock. Broadband signaling is slightly more expensive than its baseband counterpart yet still uses most of the available bandwidth; however, it does not permit the use of passive isolation taps.

Hyperchannel is a bus system that actually runs its cables onto and off of interface cards (Fig. 1)— a minor disadvantage because connecting or disconnecting a port brings the whole network down. LCN and LDDI are bus systems (Fig. 2), too, but use passive T-tap power splitters from the main trunk cable. Since trunk signals are attenuated by 11 decibels when passing from the trunk to the drop cables, the reflection caused by an unterminated one is attenuated by 22 dB, and disconnecting a port usually has no effect at all on the network's operation.

However, with Hyperchannel, LCN, and LDDI, any discontinuity along the main trunk cable may bring down the network. All three are 50-Mb/s buses, and all can operate at distances of up to 1 km at 50 Mb/s by using high-quality cable. Moreover, Network Systems Corp. offers a Hyperchannel repeater that allows it to operate at distances of up to 2 km.

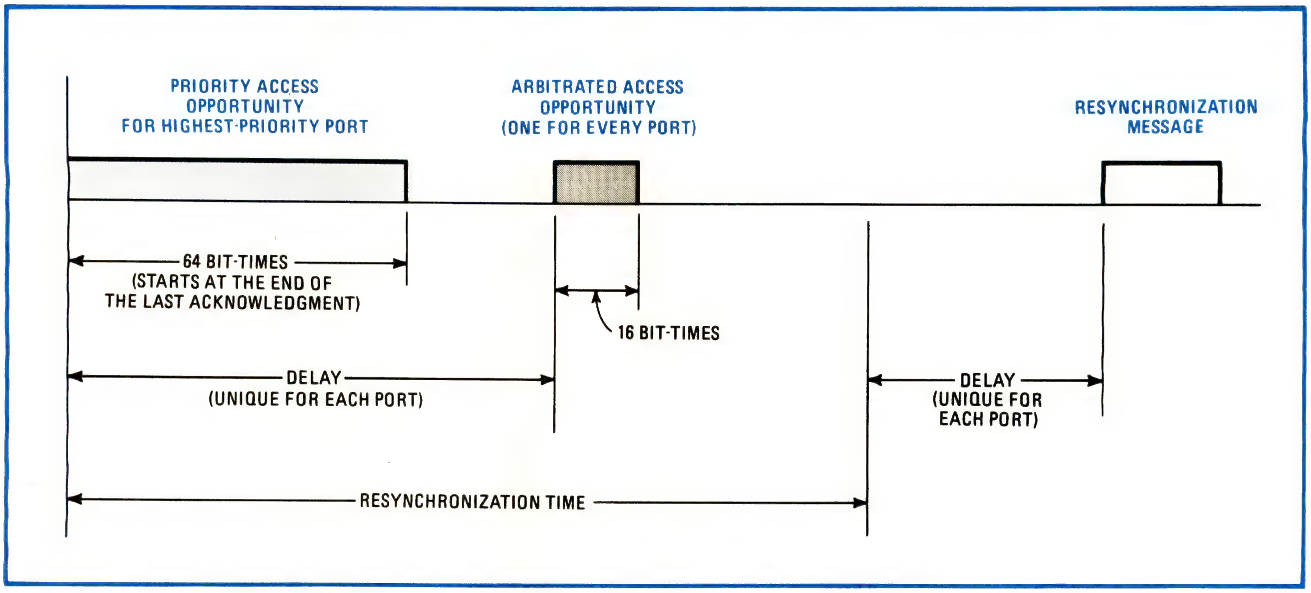
The CI uses a two-cable star topology (Fig. 3). One of the cables runs from each port to a passive star coupler—a transformer—which splits the signal 16 ways, back out to each port on a second cable. Distances are limited to no more than 45 meters from the center to a port, but the data rate is 70 Mb/s.

One advantage of this approach is the fact that disconnecting (or damaging) any cable can affect only one port. It is also rather easy to convert the CI to a fiber-optic star network with an active star coupler, since only point-to-point connections are required. T-taps and splitters, while available for optical waveguides, are generally regarded as unsatisfactory. The next generation of high-performance broadcast networks will probably use fiber optics with a two-channel star topology as well as an active center.

Physical layer

The physical-layer protocol is responsible for the fields that envelop the data-link-layer frame. All four wideband networks precede it with a preamble containing a bit-synchronizing field followed by a start-of-message code. All four follow it with a bit series that has two uses: helping to clock the last few message bits through port-receiver or message-repeater circuitry and giving the recipient enough processing time to decide whether or not to acknowledge the message. The fields range from 16 to 72 bits in length.

With a collision-avoidance arbitration scheme that is used by three out of the four networks, the CSMA protocol is strictly a physical-layer function, since only the communications medium's analog state—active as opposed to idle—is involved in arbitration. The LCN also uses CSMA/CA but employs link-layer information (a resynchronization field in the last message that is transmitted) to determine arbitration priorities. For the LCN,


PRIORITY ACCESS OPPORTUNITY FOR HIGHEST-PRIORITY PORT
ARBITRATED ACCESS OPPORTUNITY (ONE FOR EVERY PORT)
RESYNCHRONIZATION MESSAGE
64 BIT-TIMES (STARTS AT THE END OF THE LAST ACKNOWLEDGMENT)
16 BIT-TIMES
DELAY (UNIQUE FOR EACH PORT)
DELAY (UNIQUE FOR EACH PORT)
RESYNCHRONIZATION TIME

4. Bus arbitration. All wideband networks use a variation of carrier-sense multiple access with collision avoidance (CSMA/CA) for arbitration. The LDDI scheme shown is representative of all four systems: any port can transmit, but higher-priority ports get the first chance to do so.

arbitration therefore sits astride the physical and data-link layers.

When busy, all four networks work by measuring the time interval after the interconnection medium goes from the active to the idle state at the end of a transmission. All let the recipient send an acknowledgment of a message immediately after it has been received.

In each network, the port with the highest priority waits long enough to receive an acknowledgment. If the medium is still idle, the port transmits. The port with the second-highest priority gives the one with the highest priority enough time to start its message, and if the medium is still idle and there is a message to send, that port then transmits, and so on. Figure 4 illustrates arbitration as performed in the LDDI.

End to end

Hyperchannel and LDDI allow the setting of timers based on direct port-to-port propagation delays. By this means, a linear bus with n ports can be arbitrated in four end-to-end propagation delays plus n port-recognition delays, the time it takes the port to sense a change of state in the interconnection medium. Both the LCN and the CI separate ports by more than one full round-trip propagation delay. With large numbers of ports, Hyperchannel and LDDI can arbitrate more quickly than LCN or CI can; for 16 or fewer ports and less than 1 km of cable, performance differences are insignificant.

All four of the networks have a "fairness" provision that provides for round-robin scheduling when the network is heavily loaded. The provision must be used with LCN and CI, and it is optional for LDDI and usual for Hyperchannel, though adapters that do not observe fairness can be ordered for applications in which a priority structure is desired. Hyperchannel and LDDI optionally set a wait flag whenever a port transmits an arbitrated (as opposed to an acknowledgment) message. Transmission of new arbitrated messages is inhibited until every port has had an opportunity to transmit—a second timer is needed—and then the wait flag is reset. With a heavily loaded network, the effect is round-robin scheduling.

To every port, CI assigns two slots: one high priority, one low. Ports first attempt to transmit on their second (low-priority) slot. If a port with a higher priority (lower address) transmits before a port waiting for its second slot, the second port switches to its first one. Again the effect is round-robin scheduling when the network is heavily loaded.

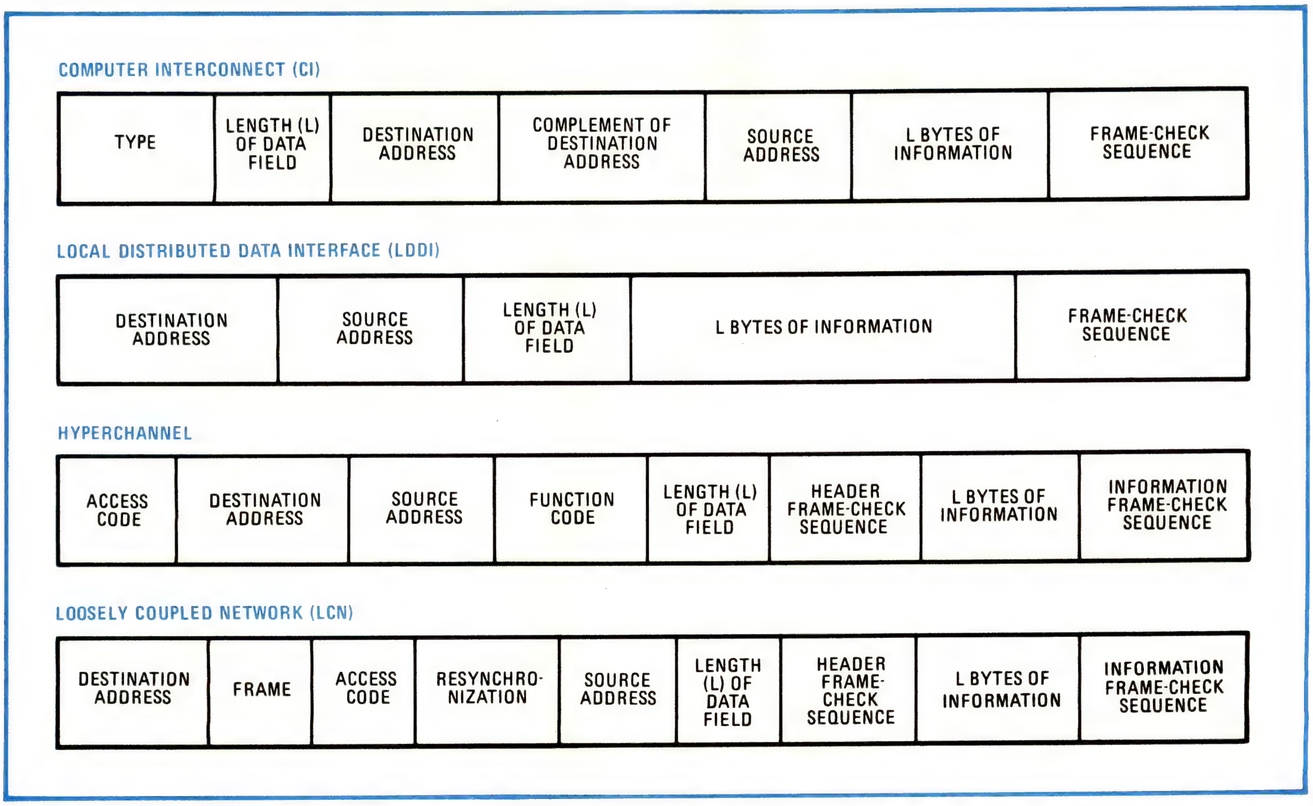
Single arbiter

One feature of the CI's arbitration is the way the arbiter ignores the cable except when it actually wants to send a packet. A single arbiter then serves two cables, and multiplexing is at the very bottom of the physical layer. Although a minor blockage results—traffic on one cable can occasionally cause a packet sent on another to be lost—this means that the incremental cost (at a port) of adding the second cable amounts only to line drivers and receivers, plus carrier-detection logic. To determine each port's priority and provide for round-robin scheduling, LCN uses a resynchronization field in the last message transmitted, and every port must store this field.

LDDI, LCN, and Hyperchannel all let two ports use the acknowledgment window at the end of frames to dedicate the network capacity to two ports for an extended dialogue. In practice, both LCN and Hyperchannel use this feature primarily when the cable serves only as a dedicated point-to-point link between a computer and a disk with a very high transfer rate.

Idle computer networks, like idle hands, are up to no good. When a CSMA/CA network is idle for a period exceeding its arbitration cycle, a strategy for continued arbitration is required.

At the end of the arbitration cycle, Hyperchannel resorts to a simple CSMA arbitration. If the cable is idle, a port that wishes to transmit does so immediately. A message collision may then occur if two ports should transmit almost simultaneously. The window of vulnera-



5. Framed. Of the four networks' data-link frames, the LDDI proposal originally included an access code like the one in the Hyperchannel and the LCN, but the X3T9.5 committee could identify no use for it.

bility to collisions is one end-to-end signal-propagation delay. Since the arbitration mode occurs only after the network has been idle for some time, collisions should be infrequent and will ordinarily be detected by the FCS at the data-link layer.

Until a CI port has a message to transmit, it pays no attention to the network's state. If the net is idle when the station first wants to transmit, it simply waits until its second slot time. If the network is still idle, it then transmits. Collisions are possible but infrequent.

LCN and LDDI pursue a different strategy, in which the active port with the highest priority is obliged to transmit a resynchronizing message after the usual arbitration period has ended. This protocol keeps the local clocks at all ports synchronized and can prevent collisions entirely, and with them the small but distinct possibility that a message damaged by a collision will pass the frame check. However, some network time is lost during resynchronization, and access times for lightly loaded networks will increase somewhat.

Network determinism

All these CSMA/CA networks can be "deterministic"; in other words, in the absence of noise, worst-case service times can be bounded absolutely. Even if collisions do occur, they cannot do so again, since the colliding messages resynchronize network arbitration.

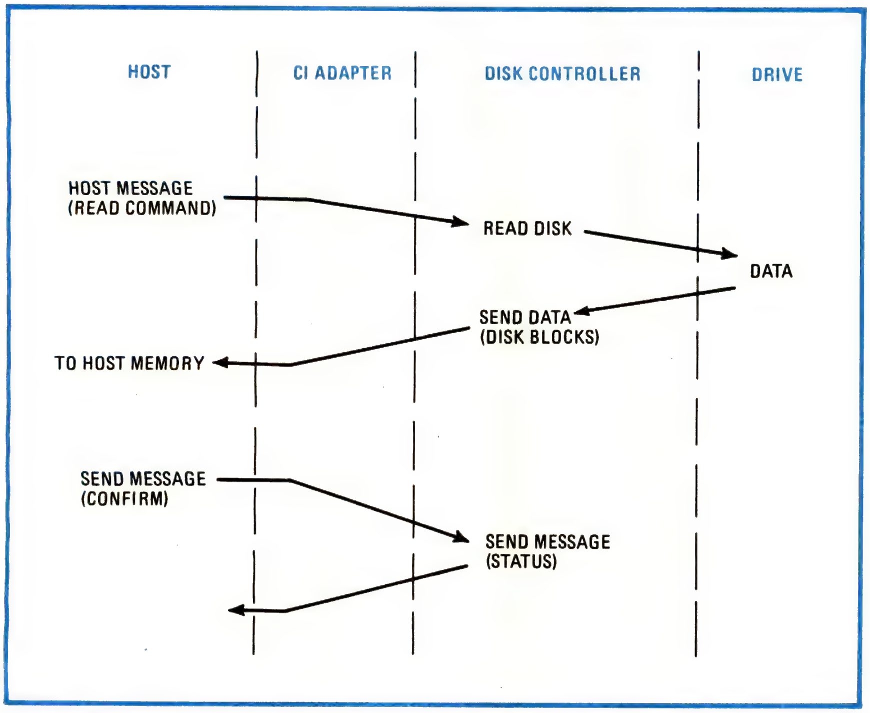
The networks have dumb data-link layers, which can be implemented conveniently in combinational and sequential logic without a programmable engine. All the networks therefore do five things at the data-link layer: during transmissions, a source address is inserted and an FCS generated; during reception, the destination address and the FCS are checked and a length field is used to define the end of the message. The LCN also extracts a field to use while arbitrating the next messages.

Figure 5 shows the four networks' data-link frames, all of which include destination and source address fields. The LDDI uses 16-bit addresses; the other networks use 8-bit ones. Since practical high-bandwidth broadcast networks have far fewer than 256 ports, a single byte suffices for link-level addressing. However, the OSI reference model uses service access points, which are addresses, to encode additional information. For instance, if the same port and data-link layer serve two different network protocols, service access points might be used. Two different addresses (service access points) would be assigned to the same port, one for each protocol.

Except for the LDDI, the networks have fields that can be used to select higher-layer protocols. The LDDI provides for this function by sticking to the OSI philosophy of using a larger address space. None of the networks makes any provision for extendable addresses or a large global (usually 48-bit) address space; all are connected to the OSI world only through protocol gateways that do not require external address mapping.

All four networks provide some sort of data-link address filtering before passing received messages to host computers. To make it easier to partition the cable into independent subnets, Hyperchannel and LCN also use an access code that can be thought of as an extension of the destination address.

All four networks also use a length field to find the end of message and the FCS. The CI has a 12-bit length



6. Handshaking. The CI has higher-level protocols that are integral with the host's operating system. It uses a confirmation send message and a status send message to flag the completion of a read from mass storage.

field; all the others use 16-bits, but the LCN length is in 16-bit words. The rest are in increments of 8-bit bytes. As a practical matter, at these data rates there is little incentive to use blocks greater than 8 kilobytes. With 1 km of cable at 50 Mb/s, there will be a round-trip propagation delay of about 500 bit times.

If an average arbitration takes eight round trips—the case for a network with eight ports and the least efficient setup for a sensible arbitration timer—arbitration takes about an order of magnitude less time than is needed to transmit a 4-kilobyte message. It should therefore be possible to use 70% to 80% of the raw transmission data rate. With 40-byte messages, a 1-kilometer network would become saturated at effective data rates of less than 5% to 10% of the raw cable bandwidth. It is the propagation delay, not the transmission rate, that limits the number of short messages on broadcast networks.

Say it again

The networks all provide for acknowledgment of all messages, chiefly to detect bad paths as they occur and if possible to use another path to reach the destination. In both CI and LCN, nonacknowledgments are sent if a message has been received properly but buffer space is not available. Acknowledgments also facilitate the retransmission of damaged messages, because a way of handling duplicate message reception should be provided when messages are retransmitted. Hyperchannel, LCN, and CI all detect duplicates.

The X3T9.5 committee has discussed the idea of allowing LDDI acknowledgment window sizes greater than one message in the network-layer protocol currently under development (in other words, the idea of using one acknowledgment message for any number of messages received). The three other networks acknowledge every message immediately. Window sizes greater than one message would facilitate longer cables and bridges to similar networks but would greatly complicate error-recovery logic. LCN, Hyperchannel, and CI all retransmit unacknowledged messages several times. If they still cannot get through, they try a different path, if one is available.

LCN sets up virtual circuits (or connections) between ports. It also provides for a data-streaming mode of operation, in which two cooperating ports, usually a central processing unit and a fast magnetic disk, hold the network for an extended period of back-and-forth messages through the tail-end acknowledgment window. Other ports (if present) never see the cable idle long enough to send an arbitrated message.

Streaming is used mainly to swap tasks in and out of main memory, to and from the disk, efficiently—without "slipping" revolutions. A 50-Mb/s trunk lets LCN keep up with a 38-Mb/s (four heads in parallel) magnetic disk.

Lock a buffer!

In Hyperchannel, the source port tells the destination port it should lock a buffer and return a message containing its control registers. The source port then sends its data message, which is acknowledged by the destination, and the source port sends a message updating the destination's control registers to indicate that a data message has been sent successfully. Since Hyperchannel supports attachment to a variety of heterogeneous computer systems and devices, a number of protocols are supported above this buffer-reservation/message-transfer level.

The CI also supports disk-read operations (Fig. 6) and four special services to the higher OSI layers:

- Send datagram. With this service, the packet is acknowledged, but successful buffering of the packet is not guaranteed. Protocols above this level suit this service as well.
- Send message. This resembles send datagram, but buffering at the destination is guaranteed or the source gets a nonacknowledge.
- Send data. The virtual address is a 32-bit process number plus a 32-bit memory address. The network layer may break long requests into shorter blocks, generally of 512 bytes.
- Request data. This service resembles send data but requests the CI to read data from memory locations in the destination node and send them to a memory address in the source.

All but the first service require the establishment of a logical connection to synchronize message serialization and permit lost, duplicate, or out-of-sequence packets to be detected. ☐

Structured methodology brings order to porting the Unix operating system

Proper organization of the programmer's development environment and new software tools are keys to successful ports

by Jeff Schriebman, *UniSoft Systems Corp., Berkeley, Calif.*

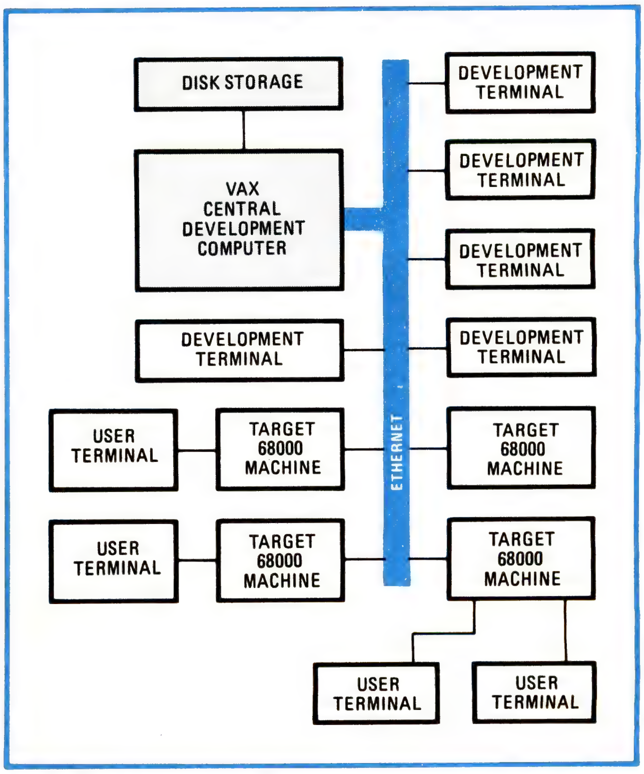
☐ Developing software is becoming an engineering task, not an art. When a methodology is put to work, it is possible to decrease the traditional 12-to-18-month development cycle and transform the programming process into a standard engineering discipline. For example, to port AT&T Bell Laboratories' Unix operating system effectively to new computers, it is important to first develop and refine standard software-engineering principles, making development as predictable as any other engineering activity. The next step is to devise software support tools that can speed the porting process. The driving force in the maturation of software engineering—the factor moving it from art to science—is the realization that using standardized management mechanisms and support tools can maximize productivity.

Any port in a storm

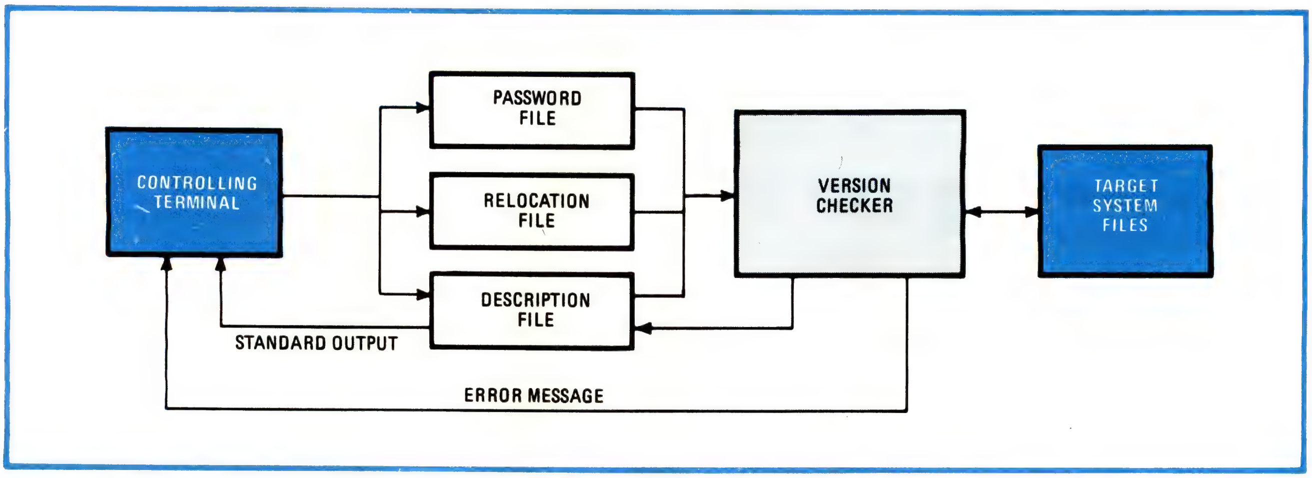
As a rule, most operating systems are written by hardware manufacturers and are machine-specific—that is, they are intimately tied to the particular hardware features of a particular machine in order to squeeze maximum speed or functionality from the software. But this intimacy makes it difficult to port the early operating systems from one computer to another. The problems of porting one of these operating systems may be as subtle as finding that an algorithm that ran especially fast on the original hardware loses speed when it is moved to the new machine. Memory management is another area where hardware tends to be intertwined with a particular operating system.

The principal impetus for porting operating systems has been users who needed to run existing software on different computers without having to recode and hence re-debug working code. Unix was created to meet these needs. The original implementation on a Digital Equipment Corp. PDP-11 was quickly followed by a port to a 32-bit Interdata 8/32; in the process, the machine-dependent portions of the operating system were identified and eliminated wherever possible. C, the language of Unix, is fundamental to the operating system's portability: although it has all the readability of a high-level language, with it the programmer can gain access to the hardware (such as registers) required to implement an operating system. The C compiler was designed for portability from the start, which simplifies the first step in porting an operating system.

Traditionally, porting is done by a hardware manufacturer interested in selling new or upgraded hardware. It is seen as part of the development process, to be done once and never again—an assumption that affects the investment in the development environment and in the software tools for the port. For instance, the architectures of the development and target machines should match, thus simplifying every process from program storage to cross-compilations. It is important for the existing and the new software to be similar as well, to further minimize the learning curve for the task. What sometimes happens, however, is that the development machine and environment are not properly suited to the task. Time is wasted creating special tools to make the development machine and target machine communicate that



1. Supportive system. Providing programmers with a supportive development environment is crucial to a successful port. UniSoft uses a VAX central development computer to download new source code quickly to targeted machines over an Ethernet network.



2. Code checker. The Vchk, or version check program, verifies that the same version of source code running on the central development computer is also running on the target machine. Such a specialized development tool should be created and maintained by a support staff.

could otherwise have been used to develop the port.

After the development system has been defined, the next step is to devise a C-language compiler to generate code for the target system, a process that can take up to six months. Some other tools also are needed, including an assembler, debugger, loader, library routines, and cross-development tools with which development can continue on one machine and testing on another.

At the same time, such machine-dependent portions of the operating system as interrupt handling and stack-mechanism and memory-management routines need to be identified and rewritten. Once the rewrite is completed—a chore that can take from three months to a year—the sources can be recompiled for the target system. Then debugging begins.

Debugging a ported operating system typically consists of performing a series of tests on the target machine, changing some code, recompiling, bringing the object code back down to the target system, and starting the loop again. Each iteration can take hours. Using disk or tape for the transfers can cause serious delays and create a bottleneck as testing proceeds.

After the operating system has been rewritten and recompiled, certain application programs must go through the same process. Interpreters, such as the one for Basic, tend to be machine-specific to maximize their run-time performance, so the source code must be reworked to optimize programs for the new environment.

New porting methodology

By applying new software technology to the problem of porting operating systems, it is possible to create a better port, and do it faster, than the traditional procedure allows. The necessary tools in a good development environment result in a less expensive and simpler port.

The classic solution to providing an adequate production environment—dedicating a large central computer to the programmers and transferring information between the mainframe and the target systems through floppy-disk drives—is inefficient. By replacing the mainframe with a network of smaller computers, work can proceed much more quickly on the target system because each new version of the software can be downloaded automatically. At UniSoft, a central DEC VAX minicomputer is networked with several 68000-based systems; the 68000s are used as targets for specific developments and as test beds for new programs (Fig. 1). All the target system needs is a small monitor program that can accept data from the network, place it in the right memory location, and start it up when the transfer is complete.

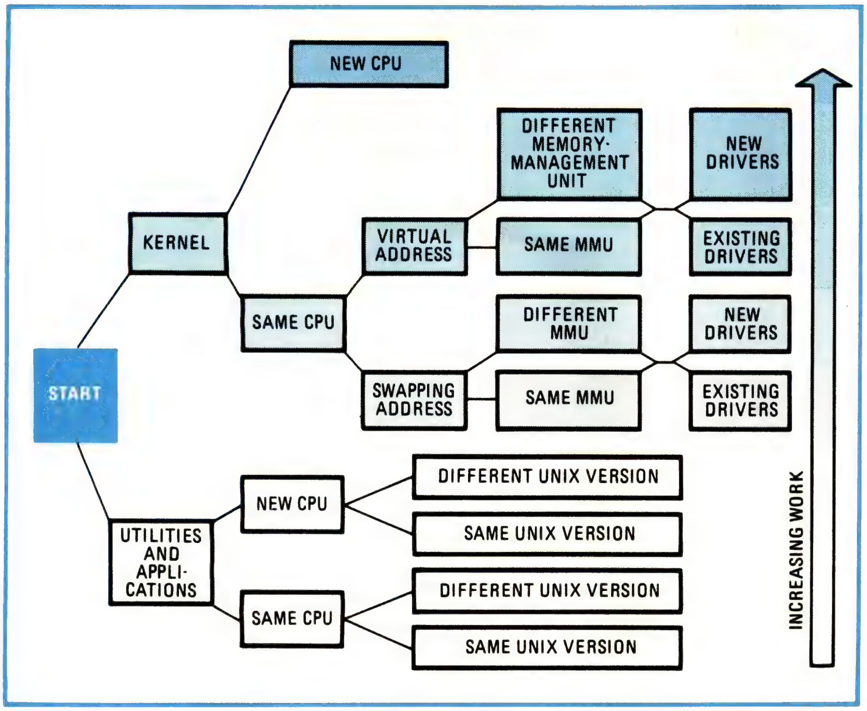
The development system should have a powerful enough central development computer and sufficient disk space for the work. In addition, it should have enough terminals to accommodate all the developers; a system programmer should never have to wait. Moreover, to keep the programmers focused on developing software, a separate group should develop the tools and handle the administration of the development system. The point is that programmers should not have to struggle with the support environment to get their work done.

A key element in UniSoft's approach is a swift and reliable file-transfer mechanism operating between the central development computer and the target machines. Two company-developed Take and Put programs are used to up- and download new source code over the network rapidly. When the programs are executed using the Ethernet networking software on the central development computer and the targets, transfers become even simpler because only a few simple commands are required to move freely among machines on the network.

To ensure that the various smaller machines networked to the central development computer pull their fair share of the load, a front-end to the C compiler automatically sends its outputs off to idle machines. This not only offloads the central development computer but also dynamically checks network integrity.

Unix comes with a number of useful support tools. Lint, a C program checker that checks parameters and types, runs on the entire operating-system source code at once and verifies that:

- All functions are called with the right numbers and types of parameters.
- All returned function values are of the right type.
- All variables are set before they are used.
- Every function is used.
- Every declared variable is used.



3. Estimating the job. The amount of time and work required for a Unix port is directly proportional to the amount of new kernel code that must be written and tested. Most new code must be developed for the memory-management units and device drivers.

In addition, Lint is a useful debugging tool when integrating new modules, such as a new device driver, into the operating system.

Another UniSoft program ensures that all ports have software identical to the central UniPlus+ source code on the central development computer. Vchk interactively checks the version and checksum of each module on a target system to see that it matches the latest version on the central computer (Fig. 2). When Vchk finds a difference between the source code on the central computer and that on the target machines, it generates the commands to get the proper modules onto the target system, thus automating a time-consuming part of the porting and support process.

Tailoring for performance

With the right development environment, powerful tools, and a standard source for the operating system, the programmer has the equipment to meet the real challenge: tailoring the operating system to match the new hardware. In 68000-based microcomputers, the main difference among Unix implementations is in the memory-management units, so any code dealing with the hardware that translates virtual addresses into physical addresses usually must be customized. Process-status commands also require customization. To handle such machine-dependent needs of the operating system, data structures in the Unix kernel have been developed that tell the program about the features of the physical landscape in the targeted system, including the type of CPU and MMU.

UniSoft, having completed a number of ports, has accumulated a library of a wide variety of device drivers. When the targeted system requires a new device driver, the programmer can look for a model in the library and use it as a starting point.

Optimizing the Unix file system improves disk and CPU throughput in any hardware configuration. The file system maintains a list of file descriptors, called i-nodes, and a chained list of free blocks onto which data can be written. To optimize the spacing of the free blocks—that is, to minimize the time it takes to allocate and access a file—three parameters can be tuned: periodicity, interleave spacing for free blocks, and logical-block size.

Preferably, periodicity is the number of sectors per cylinder, but if the controller loses time switching heads, it becomes the number of sectors per track. The interleave spacing required to handle the free blocks (called the gap) needs to be optimized to minimize the disk's average rotational latency. A new logical file system in Unix System V permits selection of either 512 bytes or 1,024 bytes. The new 1,024-byte file can improve system throughput by 15% to 30%, while imposing a modest 5% to 10% penalty in disk space, depending on the application.

The goal of any programming group is to get a product finished and delivered; yet this goal often comes into conflict with the need to chase down every little bug. Often in debugging, a bug in an operating system will turn up a bug in the compiler, which may turn up a bug in the assembler, which may turn out to have something to do with a hardware peculiarity no one had noticed. The key to a successful port is to chase down and fix every problem, no matter how slight it appears.

Scheduling software is always a thorny issue, as aphorisms such as "software is 90% done 50% of the time" and "software is, by definition, late" attest. But software schedules can be met when production software engineering is separated from development work. When the tools and techniques involved in porting are well defined, it becomes much easier to predict the time required for a successful port.

Guaranteeing the quality of new ports is much simpler with tools that ensure a common set of source code. The tailored modules—those dealing with the MMU and device drivers—are the only ones needing special checkout; the other parts of the operating system and all the utility programs have been tested previously in other implementations (Fig. 3). Another way to improve the porting process is to make the customer as self-sufficient as possible. Rather than putting forth the programmers as gurus who know all the answers, the manufacturer can invite the customer to observe the porting process and become familiar with the system. A little familiarity with the system goes a long way toward developing the confidence to take on some system maintenance. ☐

Engineer's newsletter

Robot specifications need to improve by 1990, analysis indicates

In order for robots to gain wide acceptance on the shop floor, their manufacturers must make several improvements in the near future, maintains the consulting firm, Ceeris International Inc., in a new analysis. One of Ceeris's major findings is that the rate at which robots insert components is not a key factor: **robots are most applicable in low-volume environments or for odd-form components.** When off-line programming is used, accuracy is the primary concern; cumulative tolerances of a system—not just of the robot—define real robot specifications. Packaging trends implying increased density and the increase in surface mounting also will affect accuracy. Further information can be obtained by calling (203) 434-8740 or writing to Ceeris at P. O. Box 939, Old Lyme, Conn. 07371.

Course aims to promote safe chemical handling in electronics plants

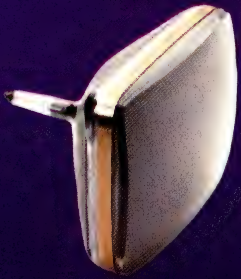
Whether a facility is turning out printed or integrated circuits, the chemicals being handled can be extremely dangerous if misused or if personnel lack proper safety training or protective equipment. So J. T. Baker Chemical Co. is giving a two-day chemical safety course for the electronics industry. **The topics include: flammables, etchants, toxic materials, insidious hazards, compressed gases, storage, labeling, and disposal**. A 275-page manual is provided to each attendee and is recommended for use in a continuing safety program at the work site. Cost of the course, which is given about 10 times per year throughout the U. S., is $350 per person. For a course at a firm's own facility, the cost must be negotiated. For details, contact Carrol Morris, J. T. Baker Chemical Co., 222 Red School Lane, Phillipsburg, N. J. 08865 or call (201) 454-2500.

Auto dashboard uses transparent plastic pc board

The climate-control panel on at least one 1984 automobile is a transparent thermoplastic printed-circuit board containing back-lit graphics and membrane switches. The board's transparent thermoplastic material is Udel (polysulfone) from Union Carbide Corp., Danbury, Conn. **Udel can offer up to 75% light transmission and will accept semiadditive electrical circuitry with plated through-holes**. The material is wave-solderable. The alternatives would have been an opaque panel with relatively high-powered incandescent lamps or expensive, complicated, and fragile light pipes.

Program analyzes data from chip tests, says NBS

The National Bureau of Standards has developed a computer program, STAT2, that can be used to analyze data from IC test structures on semiconductor wafers. **The program addresses the need to analyze, summarize, and display large amounts of data acquired using automatic test equipment.** STAT2 reads data into a two-dimensional array; calculates the mean, sample standard deviation, and median, as well as contour maps on a line printer; makes a numerical map on a terminal; makes a histogram on a line printer; and identifies spatial correlations between data sets contained in a data base. The program is written in Fortran for the standard operating system used on Digital Equipment Corp.'s VAX minicomputers, but can be adapted to other systems. To have the files necessary to build the program transferred to a user-supplied tape, contact Richard Mattis, B356 Technology Building, National Bureau of Standards, Washington, D. C. 20234. **-Jerry Lyman**



FIVRE manufactures the widest range of cathode ray tubes for data displays including panelled tubes. The application of the panel on the face of the tube is the best way to protect the operator from implosion injuries. The panel by its various antireflective finishes also offers improved contrast enhancement.

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How to make a machine act like man's

Feed it NEC's voice recognition chips.

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That's what voice recognition is all about. The user speaks. The machine recognizes his voice and executes his command. Interface is effortless, natural, completely on the user's terms.

best friend.

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COMPRESSED DP MATCHING.

NEC is a leader in voice recognition. Our economical 3-chip set forms the core of a speaker-dependent, isolated-word recognition system. Referring to voice patterns in an external 16K-byte memory, the chips respond to 128 words. More memory gives you more vocabulary: up to 512 words. Efficiency and accuracy are enhanced by NEC's exclusive compressed dynamic programming matching system.

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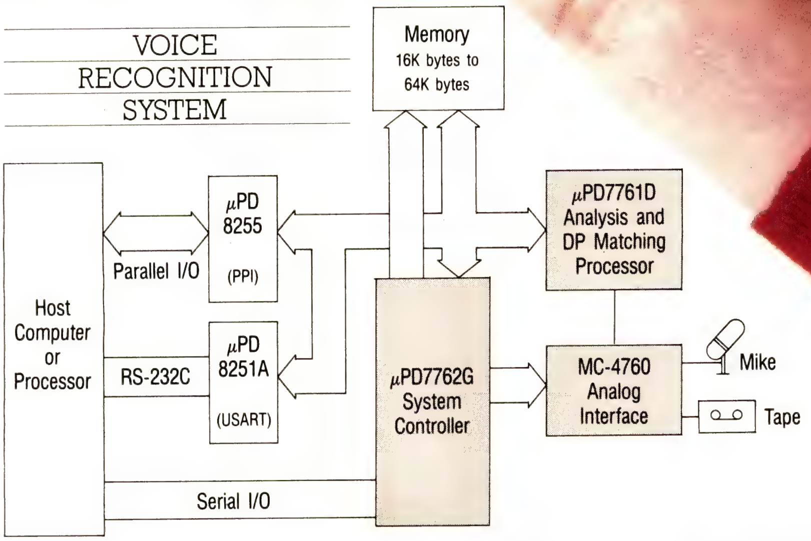

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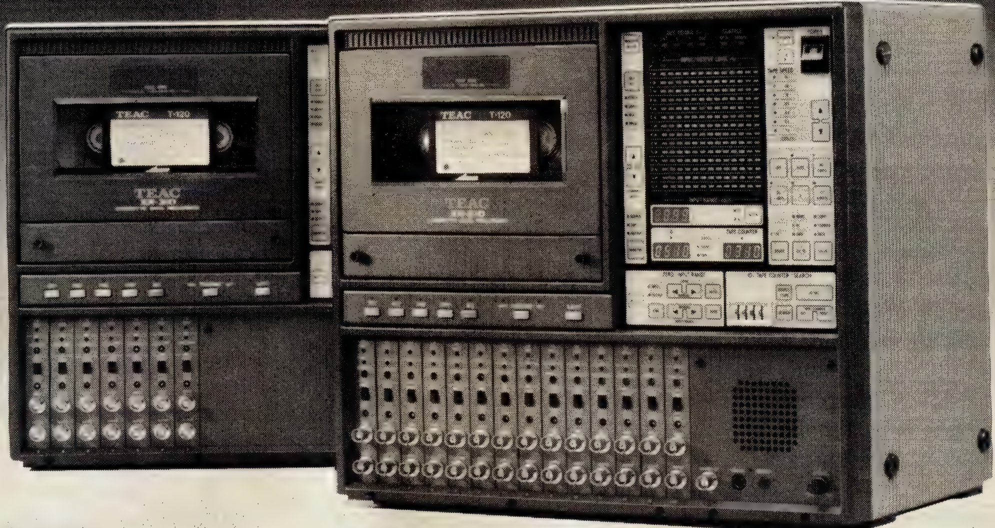

XR-30/50/70

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These three portable data recorders provide the multitrack capabilities and performance of open reel recorders with the convenience of cassette recorders. They have four selectable speeds with 8, 15, and 22 channels, respectively, and use 1/2-inch videocassette tape.

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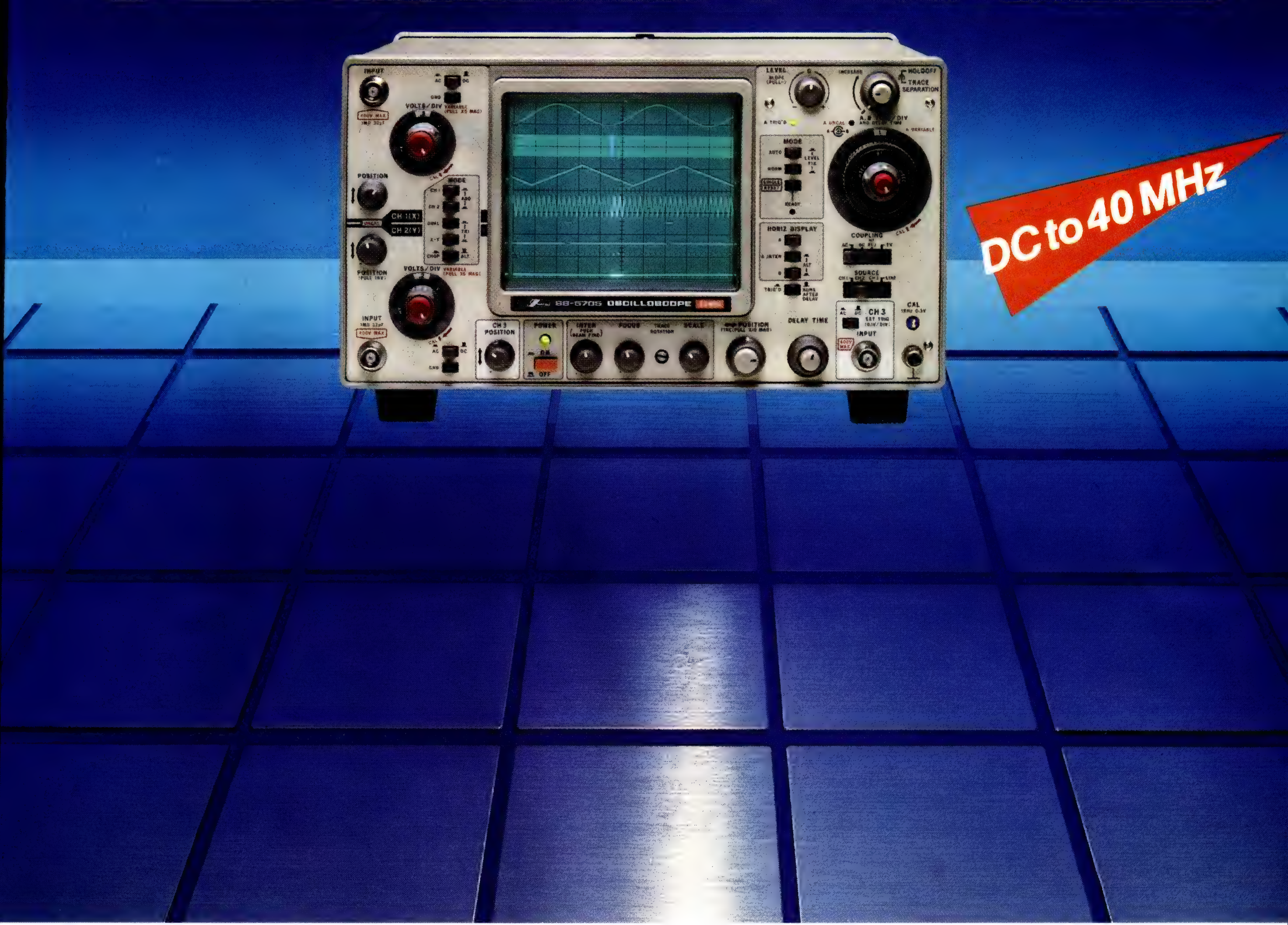

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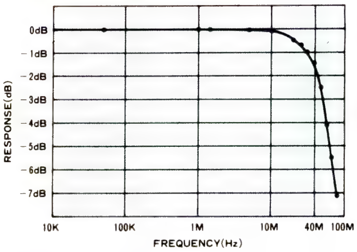

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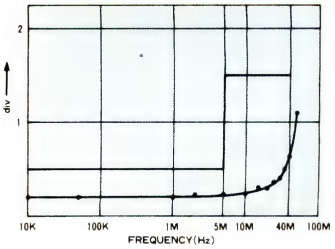

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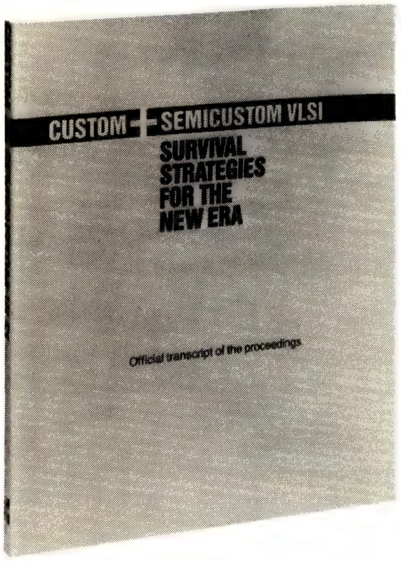
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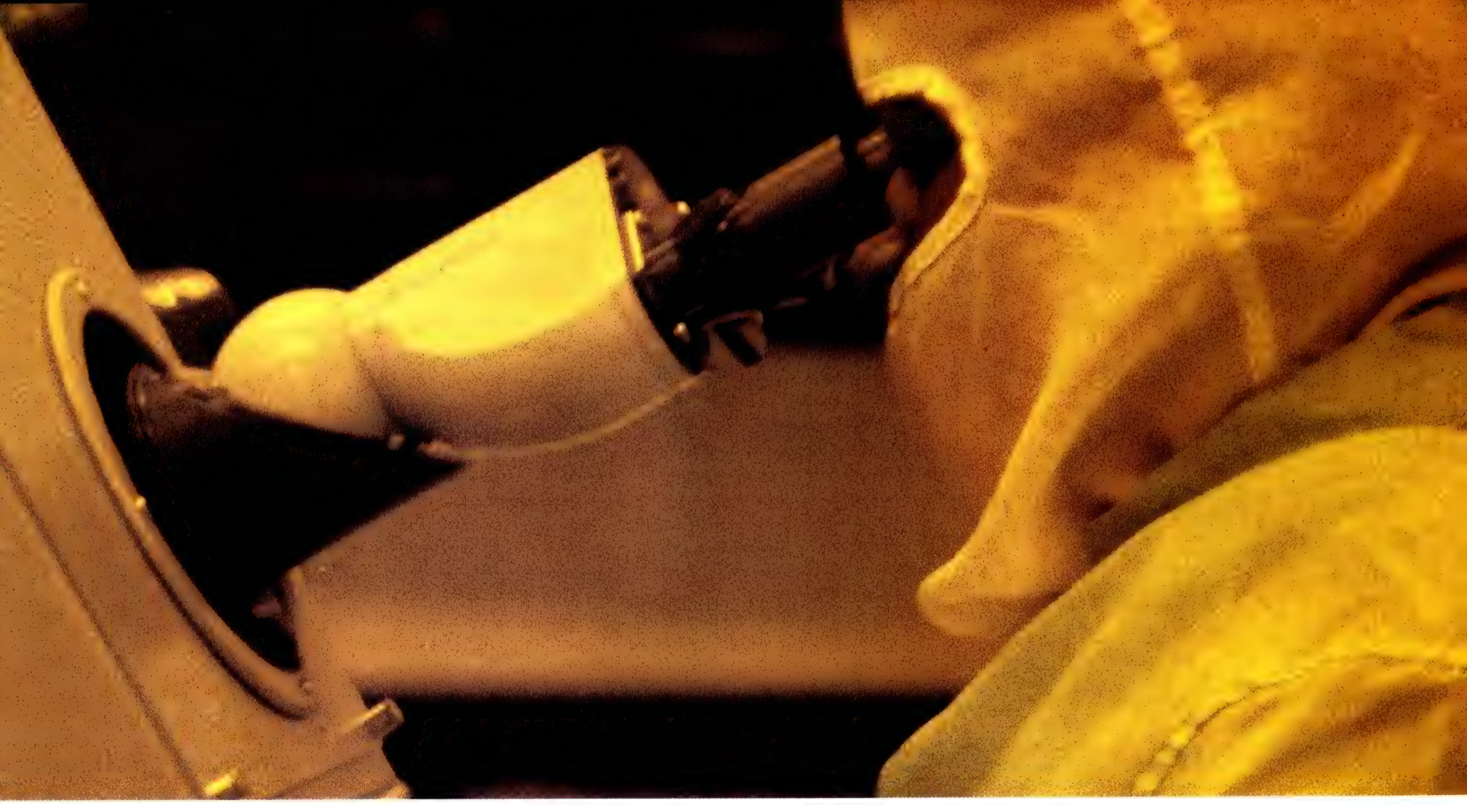

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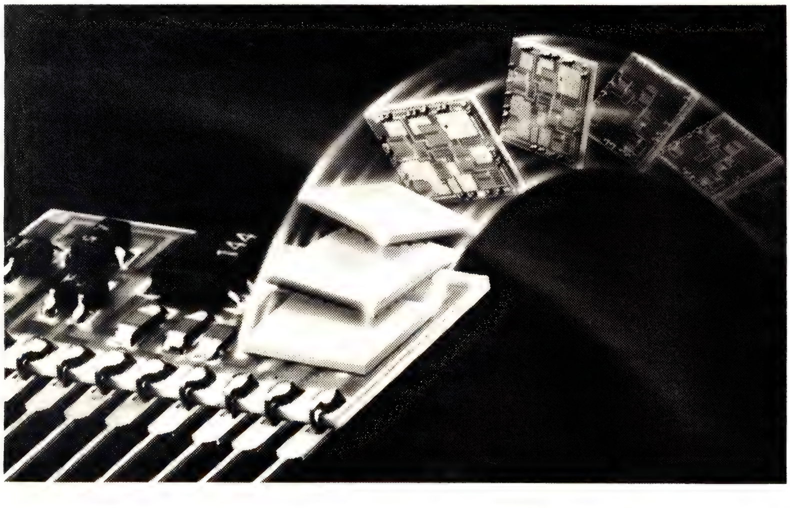
3 New Hybrid IC Technologies from Fujitsu



Unique thick-thin film combination

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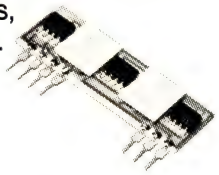
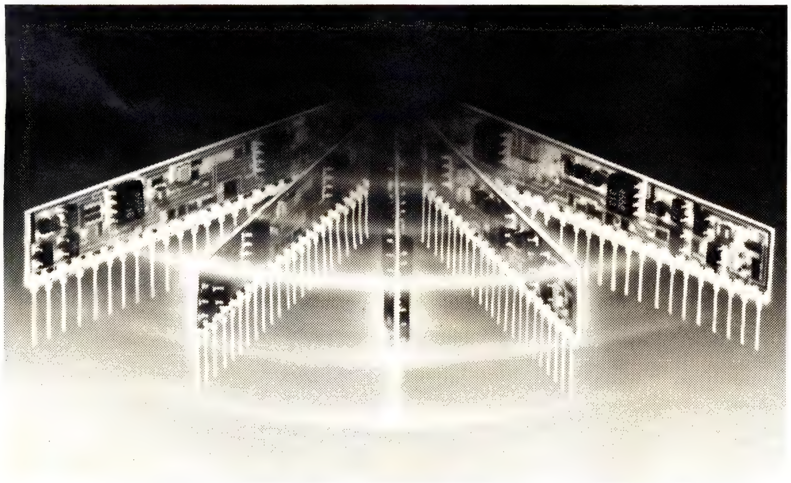
Fujitsu's T-Square hybrid IC is the result of a revolutionary advancement in the combination of hybrid thick and thin film technologies. With the choice of a thick-film or a thin-film structure for each circuit, the hybrid IC combines the low cost of thick-film circuits with the high precision of thin-film circuits in a single package. This combination is ideal for active filters, sense amplifiers, and D/A and A/D converters.

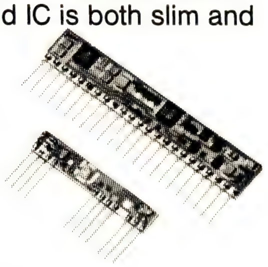


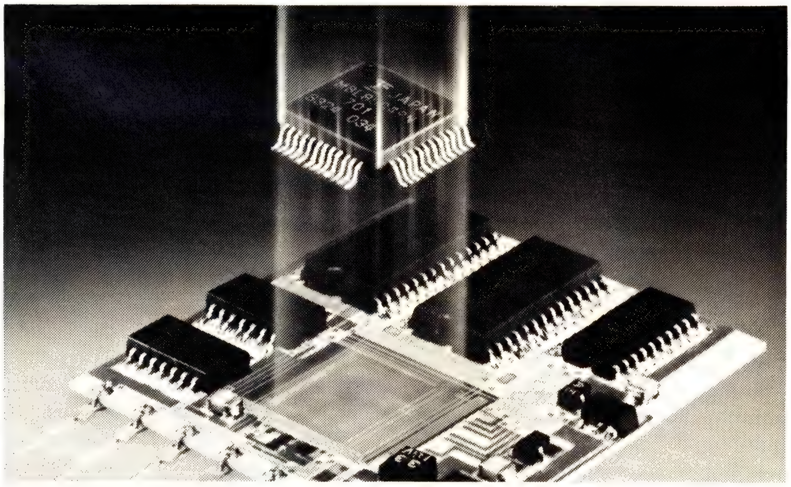


High density through double-sided packaging

Low-Profile Technology

Fujitsu pays special attention to the other side of the substrate when developing a low-profile hybrid IC. Double-sided packaging makes full use of both sides of the substrate, resulting in a low-profile IC with high packaging density. Fujitsu's low-profile hybrid IC is both slim and compact, optimum for electronics equipment that has to be thin, such as car stereos.

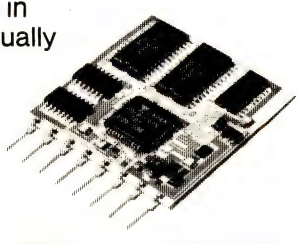




Microcomputer-mounted LSI

LSI Technology

From hybrid ICs to hybrid LSIs, Fujitsu's breakthrough in high-density hybrid IC technology is based on the integration of multilayer wiring and fine-pattern forming technologies. Fujitsu now produces a hybrid LSI where even a microprocessor, ROM and RAM are mounted. This multifold increase in capability presents virtually unlimited application potential.



FUJITSU

Fujitsu Limited·Tokyo, Japan

Fujitsu Component Europe, B.V.: Rijnkade 19B, 1382 GS, Weesp, The Netherlands, Phone: 02940-18748, Telex: 11966 FUJCENL

Circle 133 on reader service card

Electro/84

Product introductions at the Boston show include a strong round of components and shots fired on the instrumentation front

Accurate 3½-digit meter sells for only $129

Inexpensive hand-held digital multimeters, especially imported ones, are a dime a dozen. Inexpensive models with accuracies rivaling those of benchtop digital multimeters are a rarer breed. Now, however, Ballantine's 3½-digit pocket-sized model 3100A is challenging Fluke's recently introduced 70 series for the portion of the market that demands both low price and top performance.

Ballantine would like the 3100A to capture one third of the market for hand-held digital multimeters, which it pegs at over $5 million. According to Milton Lichtenstein, vice president of marketing, the low price—$129—was possible because the instrument has a low parts count and a board layout that requires minimal labor during assembly. The unit's key components are made in the U. S. and assembled in Taiwan.

The 3100A hand-held digital multimeter uses circuitry similar to the USM-451 type in the U. S. Army's 3½-digit multimeters and provides eight functions. It measures dc volts from 200 mV to 1 kV full scale, ac to 750 V, dc and ac currents from 200 μA full scale to 10 A, and resistance from 200 Ω to 20 MΩ. The unit's features include a diode-testing mode, a continuity beeper, and peak-hold capability.

The 3100A's basic dc-accuracy specification is ±0.1%, and it can measure ac signals out to 5 kHz. "The high accuracy is achieved through a stable divider network on the input attenuator," says Lichtenstein. Also contributing to this accuracy are the unit's quartz-crystal oscillator and the full shielding of its critical circuits.

For memory capabilities comparable to those of line-disturbance units that monitor power lines, the instrument's peak-hold mode goes beyond the touch-and-hold technique; it holds the peak value of transient signals in a short-term analog memory, remembering and displaying the highest positive dc or ac root-mean-square level reached by the input signal. If the signal changes to a larger value, the peak-hold memory tracks and records the change.

Surge checker. The peak-hold mode can be applied to measurements of positive-dc and -ac volts and dc and ac current. No operator interaction is required, because the mode is activated by a two-position front-panel slide switch. The peak-hold mode offers a simple way of checking ac line surges, peak-motor starting currents, and anything else where the capture of signals swinging through maximum values is desired.

The unit offers other conveniences as well. The continuity beeper makes an audible tone, indicating continuity when the unit is troubleshooting printed-circuit-board lands, tracks, cables, and circuits. The diode test function permits beta checks and accurate measurements of forward voltage drops across semiconductor diodes and transistor junctions.

The 3100A can survive a fall. Its durable plastic case has electrostatic shielding that protects it against electromagnetic interference, and it is tightly sealed to keep out dust and moisture. A combination reversible tilt stand and overhead hanger is provided on the back of the case.

A rotary switch selects all functions and ranges. To prevent damage when the unit bounces around in tool kits or in use, its switch, the meter's liquid-crystal display, and the input connectors are recessed below the unit's panel. For safety, the test leads have shrouded contacts to fit the recessed input connectors.

Overload protection is provided on all ranges. One 9-V alkaline battery will power the meter for a year's normal use. Priced at $129, the 3100A can be delivered in one week.

Ballantine Laboratories Inc., P. O. Box 97, Boonton, N. J. 07005. Phone (201) 335-0900 [Circle reader service number 346]

PROM burner taps computer for algorithms, programs both logic and memory chips

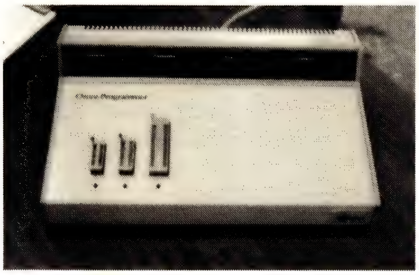
A universal logic- and memory-chip programmer from Varix Corp. handles a wide range of component types, thanks to its ability to tap into the intelligence and floppy-disk storage of personal computers.

The 3-lb Omni SP0300 can also pass along logic- and memory-programming instructions to an attached automatic chip handler for high-volume production applications. A 16-bit parallel port on the system receives chip-programming algorithms from a data base stored inside a host personal computer.

Varix is offering complete programming and development systems, bundling the Omni system with a Kaypro II portable computer with 64-K bytes of memory (making use of its two internal 8-bit parallel ports) or the 20-lb Otrona Attache unit from Otrona Advanced Systems Corp. of Boulder, Colo. Links to International Business Machines Corp.'s Personal Computer are also available in the form of host interface software, a 16-bit input/output card, and cable.

The SP0300 handles a variety of logic and storage circuits, including programmable read-only memories, erasable PROMs, nonvolatile random-access memories, programmable logic arrays, and Monolithic Memories' PALs. The front panel of the unit has three sockets—24-, 28-, and 48-pin—which accommodate standard dual in-line packages. Adapters plug into the DIP sockets, allowing the user to program components housed in chip-carriers as well as high-count pin-grid arrays.

"There are a lot of existing programming systems in the marketplace that have limited RAM capacity embedded in them, and when larger PROMs and logic chips become available, customers have to get hardware upgrades," notes Byron E. Jacobs, vice president of marketing. "Our system is virtually unlimited in memory since we use the memory space inside the host, paging programs off the disk. So the size of chip programming is limited only by the amount of disk storage."



In single quantities, the SP0300—along with the basic software but no computer interface programs or host—sells for $5,895. Complete programming systems, bundled with the Kaypro, cost $7,895. The Otrona-based Omni system will sell for under $10,000, says Jacobs. Host-computer interface software for other machines is also being provided for around $200 to $300.

Also, the Omni provides a link to volume chip handlers from Exatron Automatic Equipment of Santa Clara, Calif. The Omni plugs into Exatron's Model 2500 five-sort handler, which is also capable of burning PROMs, by a cable that plugs into one of the DIP sockets. The Varix unit passes on programming signals and control commands to the handler from the programmer, says Jacobs. This option sells for $10,995, including the handler.

Gang version. Varix is also offering a universal gang-chip programmer, the GP1140, which, like the SP0300, receives its commands from a personal computer host. However, the GP1140 can handle up to 11 chips at a time. It has a base price of $6,995.

Inside the desktop SP0300 is digital-to-analog circuitry that changes the input from the microprocessor-based host to the proper chip-programming voltage and pulse levels. The unit can drive programming-voltage levels from –5 to +30 V in 10-mV increments. The unit also contains self-calibration circuitry, eliminating the need for the user to routinely check and set the system.

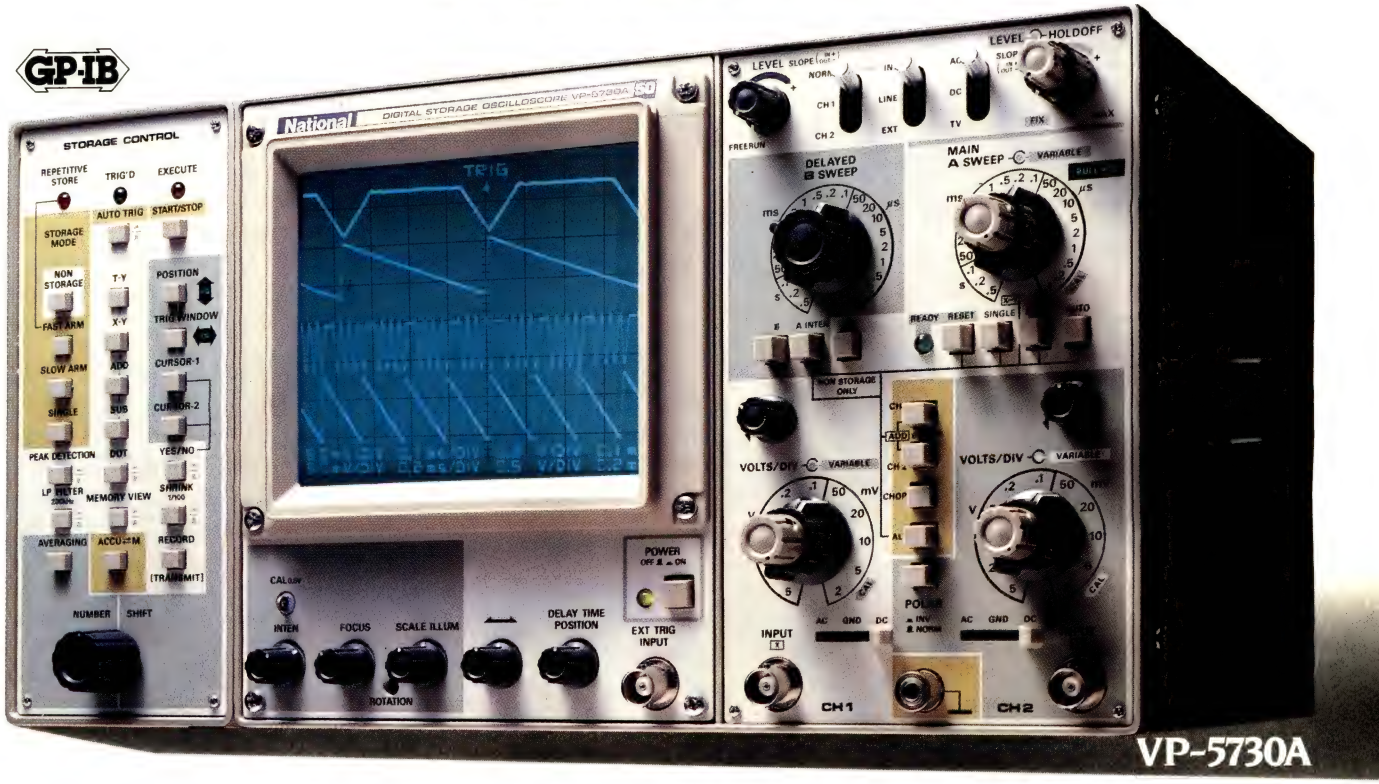
The Omni verifies the contents of the system's program buffers against the contents of the chip. If a difference exists, the system will display it on the screen of the host computer. Light-emitting diodes on the SP0300 panel also indicate errors.

Varix Corp., 122 Spanish Village #608, Dallas, Texas 75248. Phone (214) 620-0925 [Circle 343]

Set of microcomputer development tools now runs on the IBM Personal Computer

International Business Machines Corp.'s Personal Computer has become a familiar sight in engineering laboratories, where it has found increasing use in instrumentation and design applications. Seeking to take advantage of this in-place tool, Kontron Electronics, a wholly owned subsidiary of Kontron Electronik GmbH of Munich, West Germany,

THE INTELLIGENT SCOPE

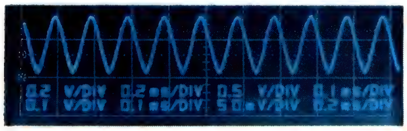


New National oscilloscope with digital display and peak detection also gives Yes/No signal judgements.

You, of course, get all the standard conveniences with the new National VP-5730A scope. But thanks to microprocessor technology, this model also thinks for you, remembers for you and even makes decisions for you.

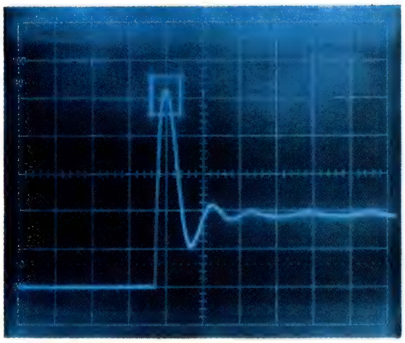
On-Screen Digital Readout

For easier measurements, the digital display shows not only measured waveforms but also trigger point, voltage and time differences with two cursor points, averaging time and other necessary information. Digitally, all at once and all on the screen.


0.2 V/DIV 0.2 ms/DIV 0.5 V/DIV 0.1 ms/DIV
0.1 V/DIV 0.1 ms/DIV 5.0 mV/DIV 0.2 ms/DIV

Clear Yes or No Decisions

Set up your own parameters with the cursors for examing input signals and your VP-5730A also gives unequivocal "OK" or "No Way" answers—fast, efficient measurements which exclude any error-prone human judgement at all.



Peak Detection and Much More

With the peak detection feature you get single-shot and repeat signals for quick identification of aliasing, fast pulses and glitches, along with clearly displayed component signal envelopes. All this plus an optional interface (GP-IB) for various system applications, an average function, storage of repetitive signals, linear interpolation in place of dots for easy reading, and much more. So make the intelligent choice in oscilloscopes. Get the model that thinks for you—the VP-5730P Intelligent Digital Oscilloscope. From National.

National/Panasonic

Matsushita Electric Trading Co., Ltd. Industrial Electronics Section, C.P.O. Box. 288, Osaka 530-91, Japan Telex: 522-8771 "METOSK J"

has adapted its universal microcomputer development tools to the PC; a hardware-and-software package lets the PC or PC XT be used as a development system for the Motorola 68000; the Intel 8086, 80186, and 80286; the Zilog Z80, Z800 and Z8000; and other popular microprocessors.

Chassis, modules. The Kontron tools—compilers, assemblers, linkers, hardware logic analyzers, in-circuit emulators, and programmable-read-only-memory programmers—have been available for use with the company's own Unix- and CP/M-based microcomputers, as well as under its older proprietary UDOS operating system. In addition, an emulator bridge allows the tools to be used with Digital Equipment Corp.'s VAX minicomputers. In each of these systems, a single chassis is mated with personality modules that adapt the system to the given microprocessor.

Kontron has now provided the hooks that make it possible to use these tools with the PC. The Kontron Development Adapter is a hardware-and-software package that adapts the PC for designing, implementing, and debugging microprocessor software; an optional emulator tests the finished package for execution on the target system.

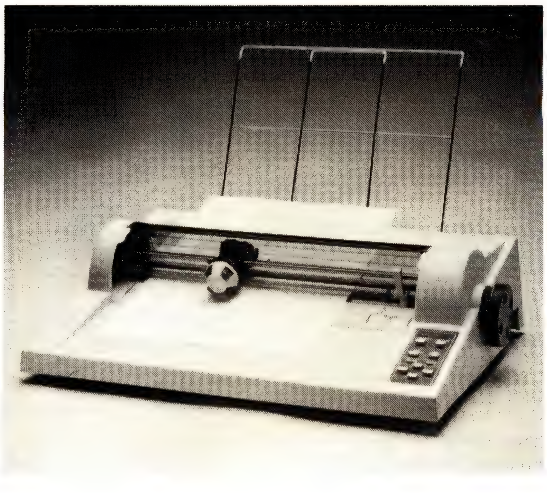
The KDA requires an IBM PC or PC XT with 256-K bytes of memory or an equivalent machine that runs MS-DOS and has an internal bus like that of the PC. Kontron says it has successfully used the system with the PC-compatible Compaq. The in-circuit emulator, which is sold separately, operates through the PC's 19.2-kilobaud RS-422 port.

The price of the KDA card with interface package to tie it into a PC is $1,500. An editor and assembler and linker software is priced at an additional $2,000.

Kontron Electronics, 630 Price Ave., Redwood City, Calif. 94063. Phone (415) 361-1012 [Circle 340]

Digital scopes get low-cost color plotter

Norland Corp. is offering a portable four-color digital plotter for use as an option with its Prowler line of digital portable oscilloscopes. The unit, to be available in 30 days, is priced at $1,900 including the necessary interface card for the Prowler. For users who have a Prowler already equipped with the card for use with other options, the price will be $150 less.



The 13.2-lb pen plotter is housed in a 16.2-by-12-by-4.4-in. cabinet and can produce hard-copy waveform information in red, blue, green, and black. The plotter, which is being provided to Norland on an original-equipment-manufacturer basis by Japan's Yokogawa Electric Works, accepts 8.5-by-11-in. paper or transparency material through a friction-feed system.

Eye grabber. Though the Prowler is offered with a 9-in. (diagonally measured) raster-scan display (with a 512-by-1,024-picture-element resolution) in a monochrome version only, the ability to produce hard copies in color will come in handy in a variety of research applications, says Garry Williams, Norland vice president for proprietary products. When used in a report, the plotter's color output will not only simplify the writing by making illustrations easier to describe, but will also serve as an eye grabber, Williams points out.

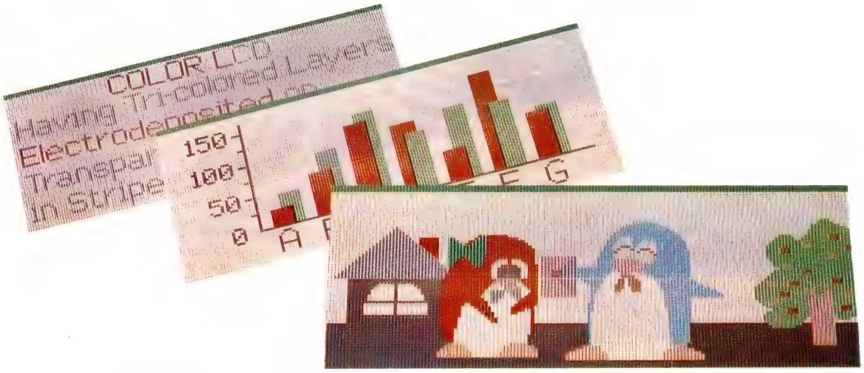
While some competitors have recently offered oscilloscopes equipped with color-display monitors, Williams says the plotter option offers Norland customers an "economical approach" to color capability short of a color display. Norland is investigating the idea of offering a color-display option later, he adds.

The user, aided by the set of 16 reconfigurable keys on the Prowler's front panel, will be able to plot waveform data in a variety of formats. Software, held in read-only memory on the interface card, allows the user to specify the color he wants plotted for the axes and various traces. Waveforms may be plotted either horizontally or vertically, for example, with one or more to a page. An entire waveform can be plotted in one color, while one or more areas of interest on that wave-

THE BIRTH OF THE BLUES...

AND THE REDS, AND THE GREENS...

In all EIGHT different colors on the world's first Multi-Color LCD Modules.



Here's something to trumpet about—the first mass-production of Multi-Color LCD Modules (LCMs). We've done it by adopting to production our newly developed CFE system (Color Filter by Electrodeposition). It's another milestone in the history of the electronic display, made possible by the experience and advanced research that makes Seiko I&E stand out in the development of LCD technology.
The new Multi-Color LCM combines a character-numeral display and color graphics to give new vividness, new expression to portable data communications.

Features:

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- Ultra-thin, lightweight. Low power consumption.
- Each module highly adaptable to varied systems.
- Custom models made on request.

Basic Specifications of Multi-Color Liquid Crystal Display Modules

Item / Model	Number of Pixels	Total Number of Dots	Display Area (mm)	Outside Dimensions (L × W × T, mm)	Display Color	Back Light
FT1616	160 × 64	480 × 64	105.6 × 42.2	170 × 100 × 20max.	8colors (Blue,Green,Red,Black, Cyan,Purple,Yellow,White)	Fluorescent Lamp
● FB2416	240 × 64	480 × 64	158 × 42	230 × 100 × 20max.	4colors (Green,Red,Black,Yellow)	Fluorescent Lamp
● FT2416	240 × 64	720 × 64	158 × 42	230 × 100 × 20max.	8colors (Blue,Green,Red,Black, Cyan,Purple,Yellow,White)	Fluorescent Lamp

● **FB2416** and **FT2416** will be available soon.

* Specifications subject to change without notice.

Basic Specifications of Dot Matrix Liquid Crystal Display Modules

Item / Model	Outside Dimensions (L × W × T, mm)	Viewing Area (mm)	Number of Display Characters	Character Size (mm)	Power Supply Voltage	Interface Format
M3212	186 × 32.8 × 9.4	147.4 × 16	32 Characters × 2 Lines	2.9 × 4.1	5.0, −5.0 *	Parallel
M3214	210 × 80 × 12.1	152 × 40	32 Characters × 4 Lines	3.50 × 5.15	6.5	Serial
M4012	186 × 32.8 × 9.4	147.4 × 16	40 Characters × 2 Lines	2.65 × 3.75	5.0, −5.0 *	Parallel
F1632	210 × 80 × 12.1	152 × 40	Full Dots	Full Dots	6.5	Serial
F2416	220 × 80 × 12.7	160 × 53	Full Dots	Full Dots	5.0 * *	—
F4816	270 × 70 × 12.7	225 × 44	Full Dots	Full Dots	5.0 * *	—
F481C	290 × 110 × 12.9	225 × 74	Full Dots	Full Dots	5.0 * *	—

* Typical Voltage of V_{LC} is -1.5V. * * Built-in temperature compensation circuit.

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form marked by cursors on the Prowler can be overprinted or printed below in different colors.

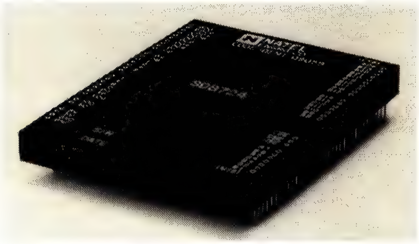
Waveforms recorded at various times can be stored and plotted later in varying colors for easy comparison. Numeric values of points on a wave may be marked with tick points and printed on the hard copy.

The Prowler, introduced at the Wescon show 18 months ago [*Electronics,* Sept. 8, 1982, p. 224], is offered in one- or two-channel versions with sampling rates of 100 kHz or 20 MHz. A single-channel 100-kHz unit offering 12-bit resolution and 4-K bytes of storage sells for about $4,000; a dual-channel 20-MHz version with 8 bits of resolution and 16-K bytes per channel goes for approximately $8,600.

Norland Corp., Norland Drive, Fort Atkinson, Wisc. 53538. Phone (800) 558-0158 or (414) 563-8456 [Circle 345]

24-bit BCD-to-binary converter is accurate to within 0.0001°, accepts 7-digit inputs

A compact BCD-to-binary converter with 24-bit resolution provides three-state outputs accurate to within 0.0001°. Natel Engineering Co.'s SDB724 converts position information received from ASCII-compatible numerical controllers to the form required by digital-to-resolver converters and position-control devices. It accepts the binary-coded-decimal digital representation of an angular displacement and provides an equivalent natural binary angular output.



Three bytes. The SDB724 accepts BCD angles up to seven digits long (359.9999°) and converts them into a 24-bit binary output with a resolution of 0.08 arc-second (±0.000022°). To interface with an 8-bit data bus, the three-state binary output is available in 3 bytes of 8 bits each. Since the BCD-to-binary conversion is entirely in digital form, it requires no timing or control signals, so its conversion is limited only by component propagation delays. The company's converter module mixes complementary-MOS and TTL components to obtain the optimum balance between power consumption and speed. To eliminate the need for special protection against electrostatic discharge, no input is connected to C-MOS chips in the module, the company says.

Typical applications for model 724 include code and format conversion in IEEE-488-based instrumentation, as well as interfacing between switches and digital-to-resolver converters. The converter's modular package measures 3 by 4 by 4 in. and weighs 6 oz. The unit costs $295 and is available from stock.

Natel Engineering Co., 4550 Runway St., Simi Valley, Calif. 93063. Phone (805) 581-3950 [Circle 350]

Chip slices data for videotex receiver

Part of a chip set that includes data-acquisition and video-generator chips, the SL9100 data slicer acts as a videotex interface and simplifies design of videotex receivers. This set is intended to receive Teletext and Prestel signals, such as those currently transmitted by station WTBS, located in Atlanta but broadcasting nationally by satellite.

Marketed by Plessey Solid State, a division of Plessey Trading Corp., the slicer accepts composite video from a standard TV receiver's intermediate-frequency detector and provides a serial Teletext data stream along with a regenerated 6.9375-MHz clock signal to Plessey's model MR9710 data-acquisition chip. It also provides a pulse to the company's model MR9735/MR9740 video generators.

An n-channel-MOS device, the SL9100 consists of an input-video buffer with a minimum input impedance of 10 kΩ feeding a chroma filter positive peak detector and a comparator. The adapter's output is compared with the output of the input-video buffer by a comparator that provides the Teletext data-stream output through a buffer amplifier. The comparator's output is also used to drive a flip-flop and 4-bit register fed by an on-chip oscillator with external crystal that reconstructs the clock signal. Pins are provided for the external overtone filter required when a third overtone crystal is used and for the external capacitors.

The Teletext data stream and clock signals provided by the SL9100 are checked by the MR9710 for a clock run-in of the correct frequency. If all is correct, the clock is bit-synchronized to the data rate with the framing code that follows, enabling byte synchronization to be performed. A serial-to-parallel converter generates the character codes that make up the Teletext message.

Provision has been made in the form of an on-chip universal asynchronous receiver-transmitter for signal reception, through an external modem, over telephone lines. Because videotex signals are asynchronous to the TV receiver, a first-in, first-out buffer is provided on chip to permit the signal to be read out synchronously by the video generators.

Video generators. The 525-line MR9740 and 625-line MR9736 interlaced video generators are functionally identical except for their line output. All three chips provide 24-row, 40-column displays and have provision for half-page expansion.

The chips also generate a boxed clock and header on Teletext and directly interface with others in Plessey's Teleview series. Also, they provide address information to the MR9710 for allocated page store and the master timing signals used by Teleview chips. All can generate a

ALL SMD'S LOOK THE SAME TO THE MDB DISK CONTROLLER

Our disk controllers can interface with any of the most popular SMD disk drives for Q-bus,* Unibus* and VAX* computer systems.

Designed to accommodate future advances in disk technology, the controller's firmware interrogates a single switch for information regarding the disk drive types in use and emulation modes. Then it automatically structures its firmware to identify the drives by number of cylinders, sectors and heads as well as number of blocks in each logical unit. Future disk technology advances may be handled by changing one inexpensive prom rather than entire firmware prom sets.

Emulating DEC's RM02, RM03, RM05 or RK06/RK07 drives, the MDB controllers are software driver and diagnostic transparent to all DEC operating systems plus UNIX** and TSX,*** without requiring any modification. Available in both Quad and Hex size boards, true, transportable media compatibility is maintained with DEC RM series drives.

MDB's SMD controller line includes models capable of handling up to 4 physical drives and 8 logical drives and capacities up to 2 gigabytes, along with a Unibus model on a single quad size board, all capable of simultaneously mixing drive types or emulation modes.

This means that over 75 different model SMD disk drives from more than 15 manufacturers are available to the DEC user without software modification.

Feature for feature you cannot mask our superiority in the field. Call us today for complete information.

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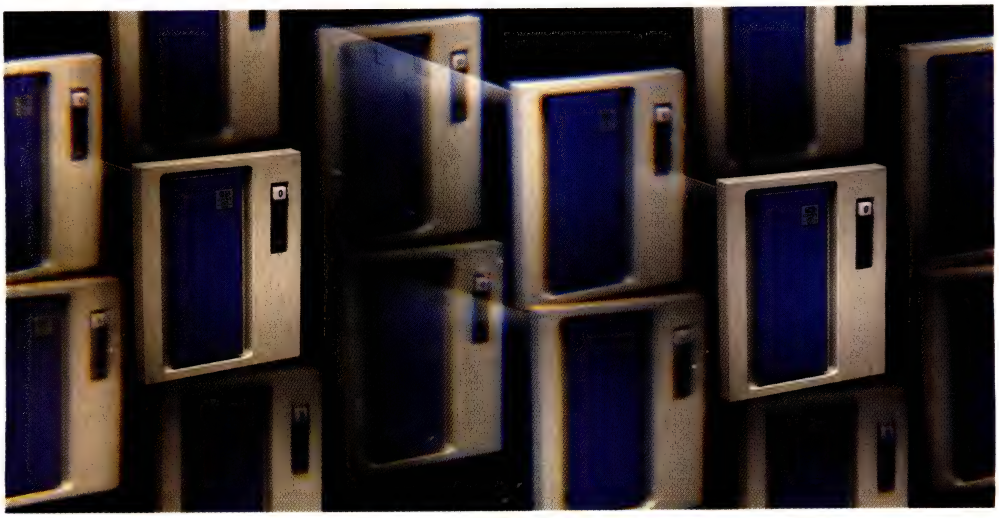

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Tel. (612) 929-6526 Telex 25631 (DULKA)
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composite synchronizing signal for reception of videotex signals, and they provide an extensive set of display utilities.

The SL9100 is housed in an 18-pin dual in-line package and requires +5 V at approximately 30 mA and ±12 V at approximately 10 mA. It operates across a 0°-to-+70°C range. Priced at $5 in lots of 100, the part is currently being sampled; volume production is planned for June.

Plessey Solid State, 1641 Kaiser Ave., Irvine, Calif. 92714 [Circle 348]

3½-digit hand-held multimeter is rugged, safe, and well protected

Safety was foremost on the minds of engineers at A. W. Sperry Instruments when they designed the DM-8010 3½-digit hand-held digital multimeter. Built for professional work in the field or in the laboratory, the DM-8010 is housed in shock-resistant plastic able to withstand the abuses of everyday service while insulating the user from shocks.

In addition, it has overload protection on all its 31 ranges. The resistance ranges, however, have solid-state protection (rather than fuses) for up to 500 V ac or dc, to protect the instrument and user from potentially dangerous misapplications. To further protect the user, test leads and their connections extending into the DM-8010 are designed to minimize exposed connections.

With a basic dc-voltage accuracy to within 0.25%, the DM-8010 DMM can read seven functions. It measures dc voltage from a range of 200 mV to 1 kV, ac voltage from 200 mV to 750 V, dc and ac currents from 20 μA to 10 A, and resistances from 20 Ω to 20 MΩ. For both ac and dc, resolution varies from ±100 μV at 200 μV to ±1 V at 1,000 V. For dc and ac currents, resolution varies from ±10 nA at 20 μA to ±10 mA at 10 A. Resistance resolution is from ±10 mΩ at 20 Ω to ±10 KΩ at 20 MΩ.

Low-power ohms. The DM-8010 comes with a built-in tilt stand, a continuity buzzer, Underwriters Laboratories 1244-type and TL-39 test leads, a diode-testing function, low-power ohms for measuring in-circuit resistance, recessed input jacks, a B-4 battery, and an F-14 fuse and a spare. It has 0.5-in. liquid-crystal-display numerals plus polarity indication, and it runs about 200 hours on a 9-V alkaline battery. A rotary switch and ac/dc selector control its functions. An ac-current jaw adapter, a high-voltage probe, and a transistor/diode test adapter are optional.

Available now, the DM-8010 is priced at $84.95.

A. W. Sperry Instruments Inc., 245 Marcus Blvd., Hauppauge, N. Y. 11788. Phone (516) 231-7050 [Circle 347]

1,000-W switcher fits in 6 by 6 by 16 in.

Building on the success of the Cool 1 series of switching power supplies, Deltron Inc. is unveiling the Cool 2 series, a family of fan-cooled, ultrareliable supplies with high power densities. They feature four to seven outputs with output-power ratings of 500 or 1,000 W. Measuring 5 by 5 by 12 in., the 500-W supply puts out 1.6 W/in^3, while the slightly larger 1,000-W unit, 6 by 6 by 16 in., puts out 1.9 W/in^3.

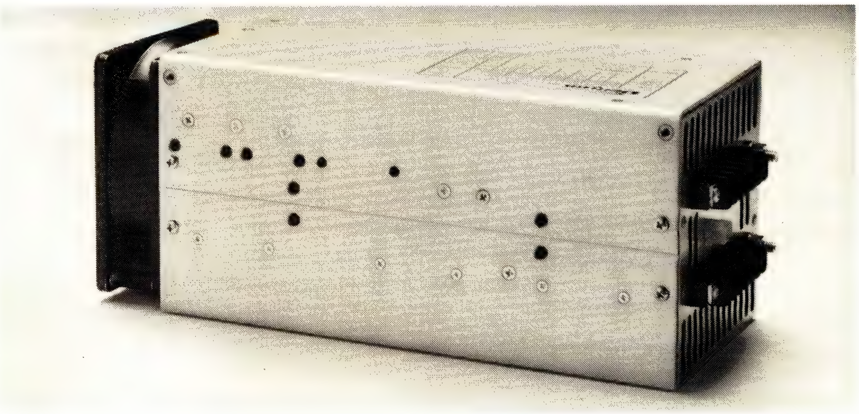
Both units have a tightly regulated main +5-V output and auxiliary outputs that are semi- or highly regulated thanks to the use of optional post-regulators. The supplies with semi-regulated auxiliaries are 75% efficient. Model Q500—the 500-W supply—has a 50-A rating on the main 5-V output. Model Q1000—the 1,000-W unit—provides 100 A on the 5-V output. Auxiliary outputs are ±12, ±15, and –24 V.

Anywhere. With input ranges of 90 to 132 or 180 to 264 V ac at 47 to 63 Hz, the closed-frame switchers are furnished for use around the world. Input surge is less than four times the steady-state peak current from cold start. A soft-start feature protects the unit's semiconductors. Both units have been designed to meet VDE 0804 and 0806 Class 1 leakage and isolation specifications, the Underwriters' Laboratories 478 standard, the Canadian Standards Association 22.2 specification, and International Electrotechnical Commission 435 and 380 Class 1 standards.

The supplies are said to have a 20-ms holdup time after loss of nominal ac power. Internal mechanisms protect them against damage for ac undervoltage operation.

Purchasers can choose among many options, including a radio-frequency interference filter to meet Federal Communications Commission standards, a line monitor, thermal shutdown circuitry, a cross-regulation minimizer, and postregulation on the auxiliary outputs. Except for the main +5-V output, polarities can be reversed.

In small quantities, the 500-W



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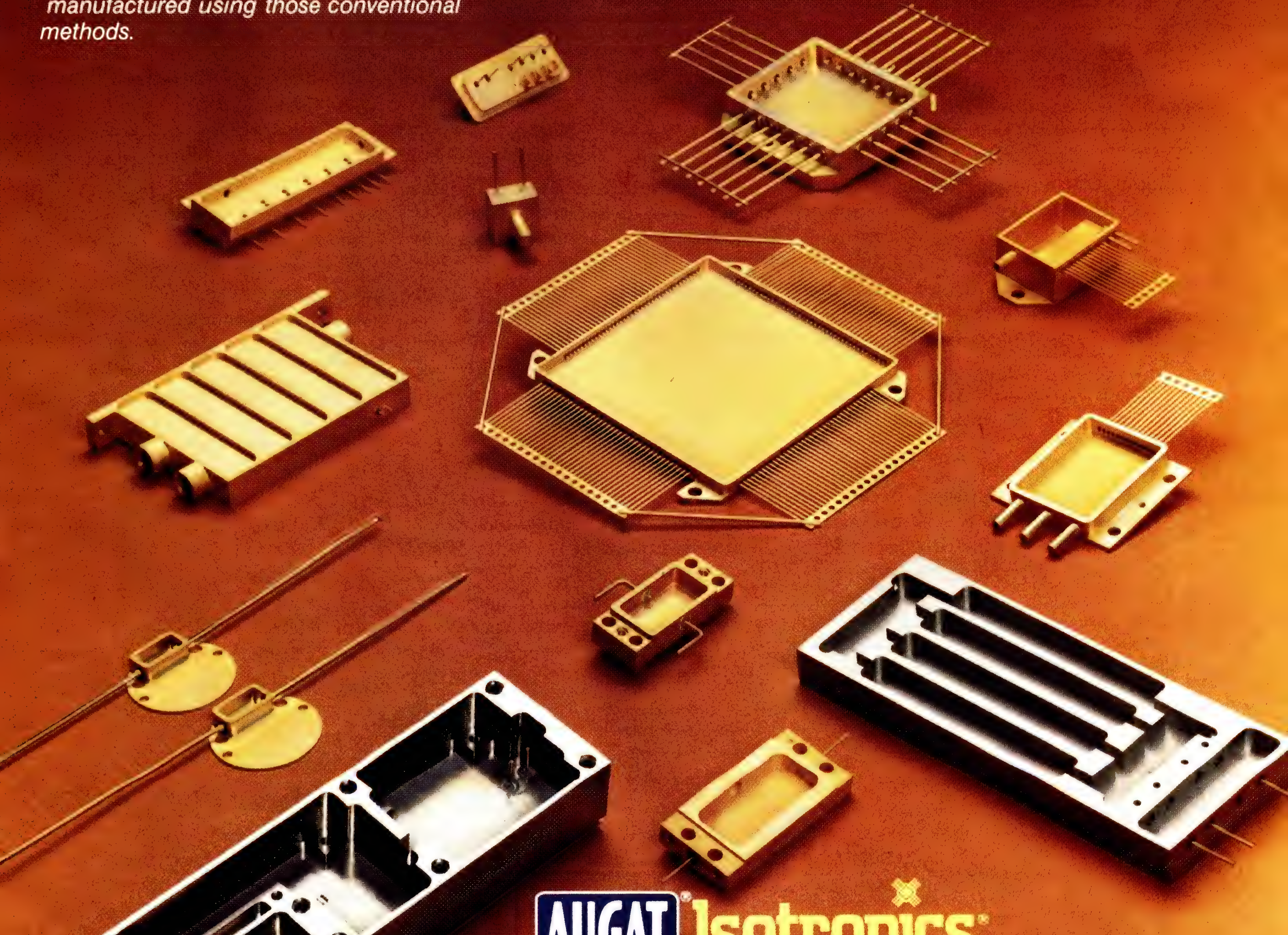

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(617)998-2000 TWX710 344 1961 Cable-Isotronics

Circle 38 on reader service card

power supply sells for $695 and the 1,000-W unit for $1,095. Both will be available 8 to 10 weeks after receipt of order.

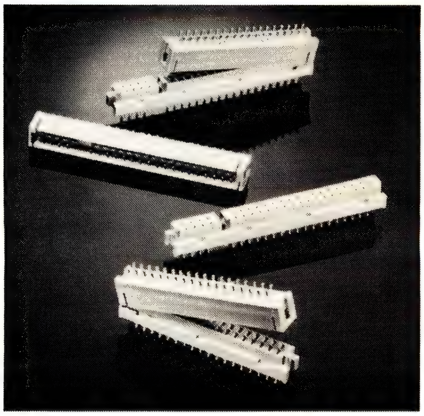
Deltron Inc., P. O. Box 1369, Wissahickon Ave., North Wales, Penn. 19454. Phone (215) 699-9261 [Circle 344]

Board-connector line gets 60-pin member

The 30/60 connector is the newest addition to Viking Connectors Inc.'s VSBX series I family of two-piece stacking connector systems. With the family of connectors, daughterboards can be stacked parallel to motherboards with a spacing of 0.5 in., permitting high-density packaging of printed-circuit boards.

The connector's 60-contact plug/receptacle brings with it a 32-bit capability along with the flexibility of adding memory lines. What's more, it incorporates the bridge concept of the series I, whereby a smaller plug can be mated to a larger receptacle. In this manner, the receptacle can mate with 36- and 44-contact plugs (for 8- and 16-bit modular boards, respectively).

Self-locking. Like the rest of series I, the 30/60 connector is compatible with board computers from Intel Corp. and National Semiconductor Corp., easing the addition of special-purpose expansion cards. The shrouded self-locking design provides mechanical support for small expansion modules, and twin cantilever beam contacts ensure an electrical interface with short current paths suited to high-speed logic applications.



Electrical operating characteristics include a current rating of 3 A maximum, dielectric withstanding voltage of 1,200 V root mean square minimum, insulation resistance of 1,000 MΩ, and contact resistance of 0.010 Ω maximum. In mechanical specifications, mating and unmating durability is said to be 200 cycles minimum. Connector mating force is 35 lbs maximum, and unmating force is 5 to 30 lbs. Contact engagement and separation force, per contact, is 1.0 to 10 oz; contact retention force is 3 lbs minimum. Its ambient-temperature range is from –55° to +122°C.

The 0.100-by-0.100-in. grid spacing and low profile suit the connector for applications that call for maximum packing density. Among these are new 32-bit mini- and microcomputers, printers and other peripherals, and telecommunications, process control, and military equipment.

In 1,000-piece quantities, prices range from 9¢ to 12¢ per contact, each of which has a 30-μin. plating of gold on the engagement area. Delivery is from stock.

Viking Connectors Inc., 21001 Nordhoff St., P. O. Box 2379, Chatsworth, Calif. 91311. Phone (213) 341-4330 [Circle 349]

Lead-acid battery made as single unit with process that eliminates gas emissions

Using a patented recombination technique that eliminates gas emissions from sealed lead-acid batteries, Gates Energy Products Inc. has just brought to market an inexpensive battery system that is fabricated as a single unit rather than built up from individual cells. The result is "a great cost-savings for customers who want to place batteries in their systems," says Ronald O. Hammel, vice president of marketing.

Dubbed the Cyclon monobloc, the rechargeable battery is targeted at a wide range of distributed power needs in electronics equipment based on sensitive integrated circuits. Monobloc batteries feature Gates's sealed design of spiraling positive and negative plates made of pure-lead grids. This configuration recombines the gases in the battery within a starved electrolyte system.

Near delicate parts. "Because the battery recombines a majority of the gases that are given off in overcharge, there is no emission of corrosive vapors into the atmosphere," Hammel says. Thus the unit can be placed next to solid-state memories and other delicate components.

"The distribution of power through networks of smaller batteries is a growing trend in a number of systems," Hammel notes. "This way, one failure will not impact the entire system." The monobloc is also suited for a number of low-power complementary-MOS applications, including telecommunications, portable computers, instrumentation equipment, and mobile robots.

Initially available in two basic sizes—2.5- and 5-A-h capacities in 4- or 6-V modules—the monobloc provides a float-life (where the battery is placed on continuous charge until needed) of up to 8 to 10 years at 23°C; its cycle duty (where the battery is used and then charged) is said to be 200 to 2,000 h. In quantities of 50,000, the 6-V, 2.5-A-h system sells for $5.16 each.

Gates Energy Products Inc., 1050 S. Broadway, P. O. Box 5887, Denver, Colo. 80217. Phone (303) 744-4806 [Circle 342]

Ribbon connector uses 0.025-in. centers

By developing a D-shaped insulation-displacement connector with 0.025-in. centers for flat-ribbon cable, ITT Corp.'s ITT Cannon division has reduced the size of the miniature workhorse connector by 50%. Current connectors of this type all make use

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Military Nomenclature:
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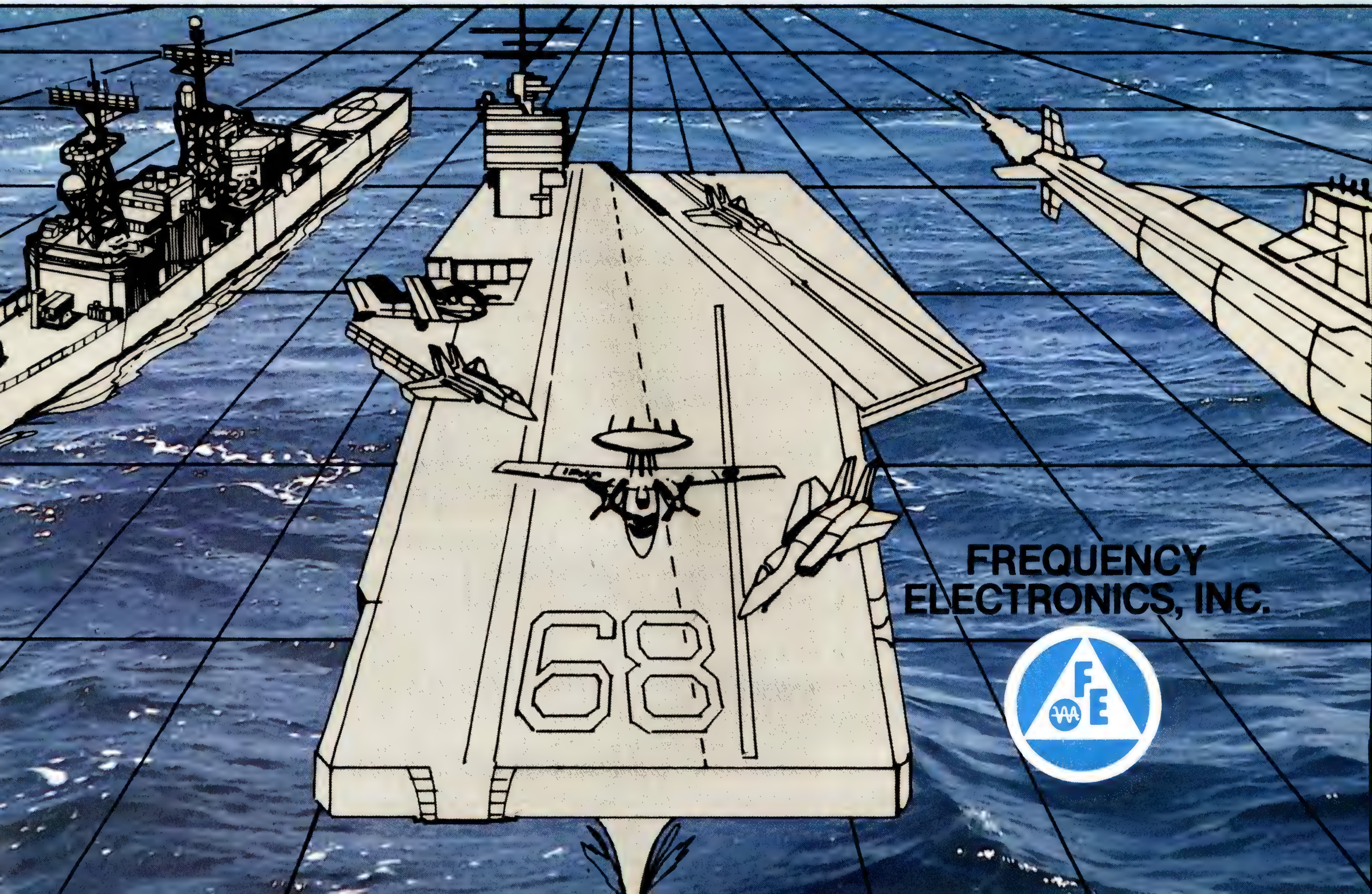

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DISCHARGE TUBE
FOR CIRCUIT PROTECTION

TYPE SA-7K
(Actual size)

• TYPE

Type	Breakdown Voltage (V) D	Insulation Resistance (Ω)	Maximum Surge Current (8×20us) KA	Life Times at 500A
SA-80SS	80±10%	10^{10} min	1.0	1000
SA-200SS	200±10%	10^{10} min	1.0	1000
SA-80	80±10%	10^{10} min	1.5	3000
SA-140	140±10%	10^{10} min	1.5	3000
SA-200	200±10%	10^{10} min	1.5	3000
SA-250	250±10%	10^{10} min	1.5	3000
SA-300	300±10%	10^{10} min	1.5	3000
SA-7K	7000±1000V	10^{10} min	—	5000
SA-10K	10000±1000V	10^{10} min	—	5000
SA-180D(3)	180±10%	10^{10} min	2.5	10000

SA-180D(3) is a three electrode discharge tube.
All tubes can be made dark effect redused types which are available upon request. D is added to the model number, as in SA-80DSS.

• POINT

(1)Usable at wider ambient condition, especially good under high humidity.
(2)Visibility for operation.
(3)Compact and easy assembly.
(4)Stable characteristics.

• APPLICATION

Computer circuit.
Communication equipment.
Home Appliance.
Aircraft and Automobiles.

TYPE
SA-80SS
(Actual size)

MAIN PRODUCT
NEON GLOW LAMP, XENON FLASH LAMP,
RARE GAS DISCHARGE LAMP
MINIATURE: BLACK-LIGHT, UV-LIGHT,
FLUORESCENT COLOR-LIGHT.

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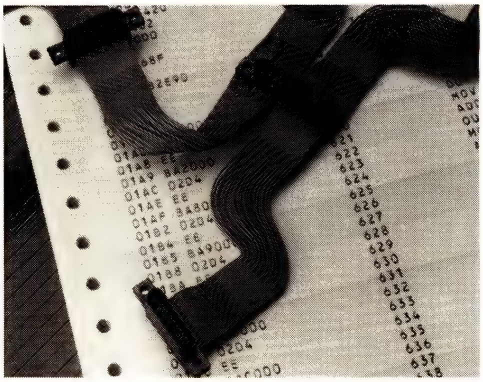


of 0.050-in. cable spacing.

The Micro/IDC connector helps designers of miniaturized computer and telecommunications systems achieve higher pin densities in smaller packages. It and the density improvement cut "cable volume and weight, along with the printed-circuit-board space requirements, by up to 50%," says Darrell Hadley, marketing manager of ITT Cannon's Microminiature/Fiber-Optics division, in Santa Ana, Calif. The connector is meant to accommodate the increasing use of very large-scale integrated circuits, which need more and more input/output lines, he adds.

The Micro/IDC is compatible with standard microconnectors on 0.050-in. centers and mates with the ITT Cannon twist-pin connector. Users therefore do not have to change connector halves to employ the flat cable with 0.025-in. centers. It is available in six contact configurations: 9, 15, 21, 25, 31, and 37, as well as in three versions: the Micro/IDC alone, with the cable, or with cable harness. Termination equipment is available.

In fact, a major benefit of the Micro/IDC is the ease of terminating it. Users can do so themselves, "which lowers the total package cost," Hadley notes. The task can be done with an arbor-type press in seconds and does not require extensive training. The connector can also be terminated with either polyvinylchloride or Teflon cable. PVC is recommended for applications where temperatures are moderate, Teflon for use in hotter, more hostile environments.

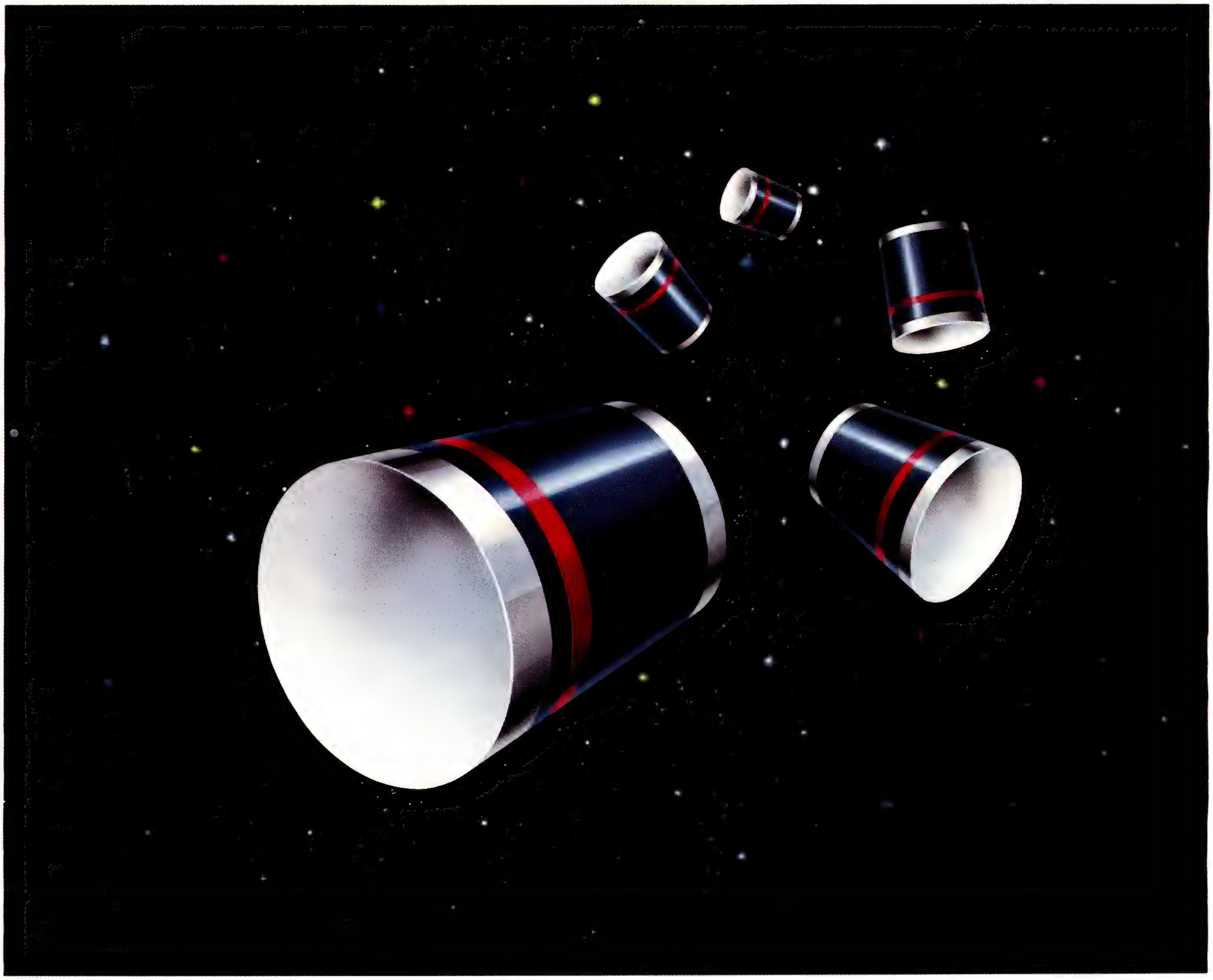
Selective plating. Hadley says the connector was designed to be relatively inexpensive, a goal "achieved by using a stamped contact, selective plating, and volume production." Priced at $12.33 in lots of 1,000, the Micro/IDC is available with standard lead times of four to six weeks.

ITT Cannon, 10550 Talbert Ave., P. O. Box 8040, Fountain Valley, Calif., 92708. Phone (714) 964-7400 [Circle 351]

Light-emitting diodes put out 160 mcd, are housed in four-element arrays

Dialight Corp.'s Superbright line of light-emitting-diode indicators, so named because lamps can be had with intensities of up to 160 millicandelas, is getting three new series: four-element arrays, snap-in indicators, and circuit-board indicators. All come in four colors—red, green, yel-

Our surface mount SUPERECTIFIER® has redefined the concept of time and space.



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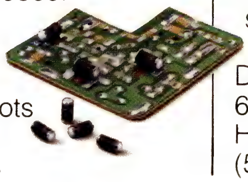

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(516) 733-3333.

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low, and amber—in either diffused or water-clear packages.

All the parts, which dissipate 125 mw (100 mw for the red LEDs), range in intensity from 12 mcd for green diffused models to 160 mcd for red and yellow clear parts. The LED's angle of half intensity is from 20° for clear amber parts to 70° for diffused red models.

Four-element arrays for use on printed-circuit boards make up the 550 line. The TTL-compatible arrays have four T-1¾ LEDs mounted in a compact black case. With the four elements in one package, designers can satisfy requirements for multiple lamps at a minimum cost. Also, the multiple light arrays facilitate positive seating and spacing.

The arrays, which are compatible with the firm's 550 series of individual units, have separately accessible leads for each element and pretrimmed leads for board mounting. Wave soldering can be used to mount them on the boards. Priced at $2.72 in lots over 100, the four-element arrays are available now, with delivery taking about three weeks.

Snap-in models. The 559 series of snap-in indicators can be mounted on 0.300-in. centers on panels from 0.031 to 0.062 in. in thickness. Suitable for computers, instruments, communications gear, and medical equipment, the LEDs need no extra hardware. Their straight terminals are suitable for wire wrapping or soldering. Small-quantity prices are $1.46 each for the straight terminal type and $1.86 each for those with varying-length wire leads. The LEDs can be delivered in three weeks.

The last of the line's additions is the 561 series of circuit-board indicators, available in six heights. A spacer, which provides for exact alignment during wave soldering, holds the LED firmly; no additional fixturing or gluing is needed. For correct electrical connections, the LED's cathode is clearly identified. In lots of 100 or more, members of the 561 series sell for 76¢ each and are available in three weeks.

Dialight Corp., 203 Harrison Place, Brooklyn, N. Y. 11237. Phone (212) 497-7600

[Circle 352]

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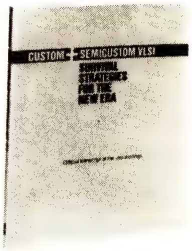

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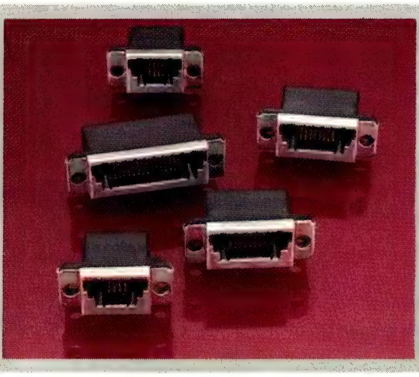

Top or side entry pcb receptacles, for complete design flexibility.

Round shielded cable terminates in just two steps– one for the conductors, one for the shield.

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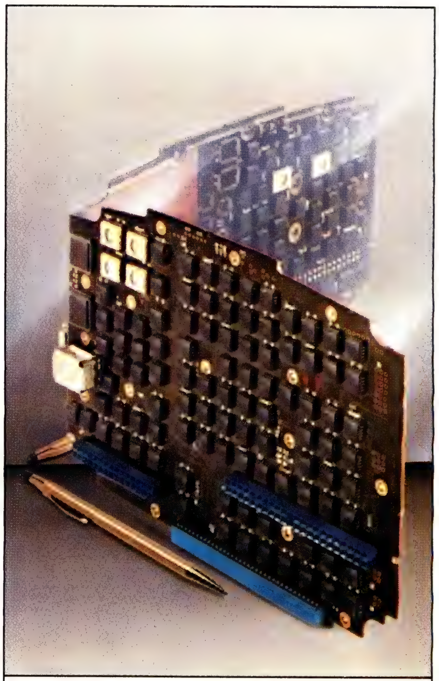
Texas make

As Collins Avionics and Singer-Kearfott developed JTIDS*, the new communications system for the F-15 fighter, Texas Instruments helped solve a severe circuitry packaging problem.

The new system utilizes the most advanced chip packaging technology, the



Successful application of high-density packaging was achieved in the PC boards of the F-15's new communications equipment. TI's clad metal system solved thermal expansion mismatch. This mirror-reflection photo shows how ICs were mounted on both sides of the PC boards.

leadless chip carrier. Design objectives called for 191 components to be surface mounted on both sides of a 6″ × 8.5″ printed circuit (PC)* board—and to dissipate up to 40 watts of power.

But, during thermal cycling tests, the difference in the thermal coefficient of expansion (TCE) between the ceramic chip carriers and the conventional PC

◀ **Improved reliability** in the F-15's new communications system (JTIDS) is achieved with TI's copper-clad Invar used to prevent solder joint breakage on densely populated PC boards. TI teamed up with Collins Avionics and Singer-Kearfott to meet the demanding packaging requirements of the fighter's receiver/transmitter.

---

*Joint Tactical Information Distribution System

Instruments and Collins Avionics dense circuit reliability soar.

board caused the solder joints attaching the components to the board to break.

TI's solution: A composite metal core of low-TCE Invar that is clad on both sides with copper. Thin, polyimide-glass, multilayer boards were bonded to each side of the metal, to provide the circuitry function.

With a TCE match between the board and the chip carriers, the PC boards easily passed the exacting thermal cycling tests.

And the metal core in the board dramatically improved thermal conductivity and overall rigidity.

Solves thermal mismatch problems

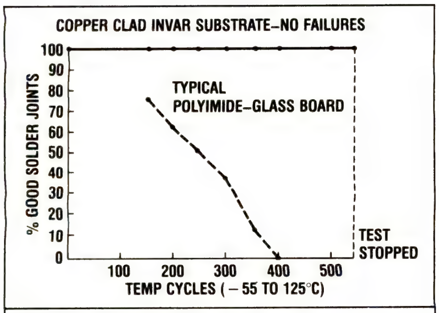
As Collins Avionics discovered, the advantage of using chip carriers to achieve high-density, high-performance circuitry also imposes stringent demands for increased thermal management, structural integrity, as well as TCE compatibility—demands met by Texas Instruments copper-clad Invar.

By combining TCE compatibility with high lateral thermal conductivity. And mechanical rigidity.

All at lower cost than alternate approaches. ■

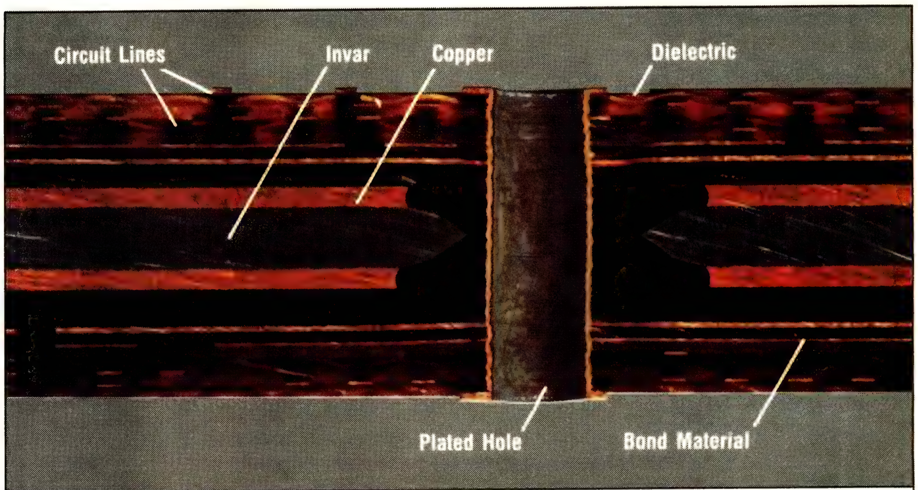
The solution is a trilayer metal.

TI's process involves roll bonding copper foil to Invar—a 36% nickel/64% iron alloy. The bonding to each side of the Invar is accomplished by the same process used to make thermostat metal and coins. No adhesives or brazing alloys are required to achieve a permanent bond.



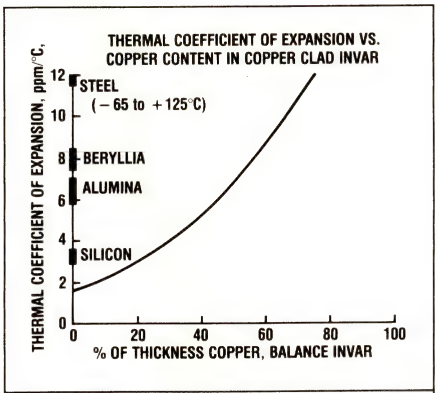
After 540 thermal cycles from −55° to 125°C failed to break chip carrier solder joints, Collins Avionics halted tests of PC board used in F-15 communications system. Reliability goals had been surpassed by a wide margin.

©1983 TI 27-9216



Effective thermal management is achieved with a copper-clad Invar core that acts as a support for circuitry in the PC board. Heat dissipation characteristics of the copper are excellent, and the Invar contributes rigidity and strength.

By varying the ratios of the high thermal conductivity copper to the ultra-low TCE Invar, the TCE of the clad metal can be tailored to match that of silicon, alumina, or beryllia.



Matching the TCE of the metal core of a PC board to chip carrier ceramic is accomplished by bonding the correct ratio of copper to Invar.

This material is available in thicknesses from 5 to 62 mils (.13 to 1.57 mm). You can get it in widths up to 24 inches (610 mm).

Copper-clad Invar is being developed for many other applications: From ground and power planes in multilayer boards, to heat sinks and covers for multichip ceramic modules, and more.

A clad remedy to packaging challenges

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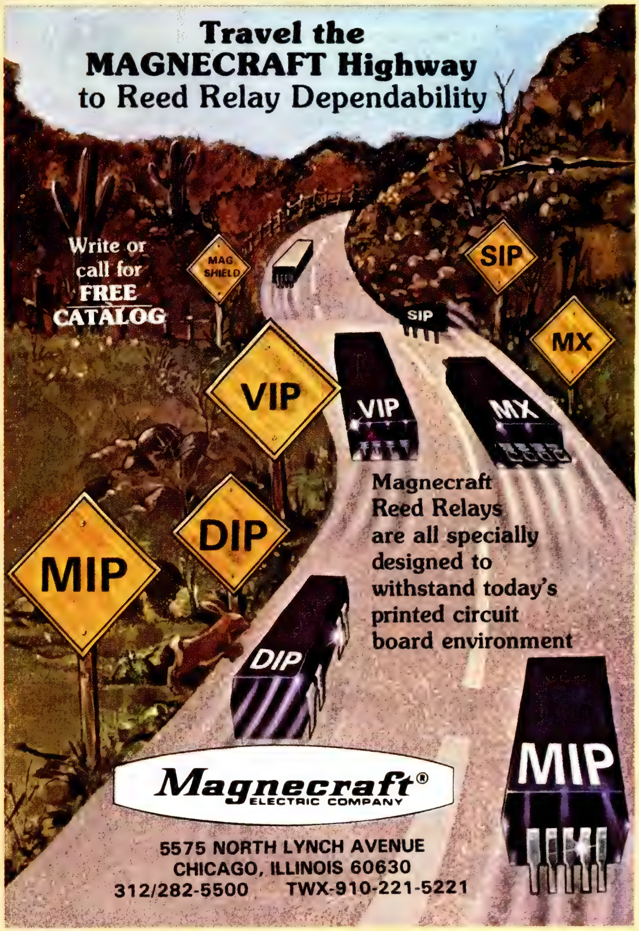

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System displays 1,664 by 1,248 pixels

Work station combines high-resolution fast color graphics with 32032-based subsystem for design and simulation

by Steve Zollo, New Products Editor

Although early graphics systems promised much, they performed poorly—especially when taxed with complex applications. Targeting high-level computer-aided-design and -engineering, Saber Technology's Interactive Graphics Computer System (IGCS) tackles what the firm regards as the shortfalls of those systems.

L. A. Dorie, Saber's vice president of marketing, says that their current deficiencies include "too low a resolution, which is often made up for by various anti-aliasing techniques; low brightness, compensated for by darkened rooms; flicker, frequently minimized by use of incandesent lights instead of flourescent; and big physical dimensions."

Saber's new video-monitor technology, which according to Dorie offers higher resolution and faster graphics than competitors do, is the system's heart. The IGCS is backed by a NS32032-based processing subsystem that uses AT&T Bell Laboratories' Unix operating system. Saber has created a fast, state-of-the art machine that makes current rivals look slow and inefficient, says Dorie.

Small, sharp pixels. Believing that a high-quality video monitor is the single most important component of a CAD/CAE setup, Saber took current technology and improved on it. The firm's own patented Q-SEL amplifier circuit helps provide very sharp, clear picture elements by putting more energy on screen in a smaller spot. In fact, the display is bright enough to be used in offices with fluorescent lights.

With its proprietary advanced display circuit technology, Saber has achieved both monochrome and color resolutions of 1,664 by 1,248 pixels—2 million pixels on screen with a 60-Hz noninterlaced refresh rate and full grey scale.

The screen measures 19 in. across diagonally, which is regarded as the optimum size for CAD/CAE—that is, the largest one that does not force head movement at the typical viewing distance of 18 in. Another advantage of the IGCS is its small footprint, for convenient desktop use.

The screen's brightness, speed, and resolution are fully exploited in Saber's graphics subsystem. A full screen can be filled in less than 1 s. The image memory has 2 Mb of memory per plane, and there are two planes per board. A total of four boards or planes of memory can be accommodated—and an additional eight in an expanded chassis, for a total of 24 planes that can be used for different layers of an image or to generate 16 million colors.

For the brains of the IGCS, Saber turned to National Semiconductor's 32-bit 32032 microprocessor, a five-chip set including, besides the processing unit, the following peripherals: the floating-point unit, a memory-management unit that supports demand-paged virtual memory operations, a timing control unit, and interrupt control unit. Running at 10 MHz, the processor can deal with about 1.2 million instructions/s, and the system can use two such processors. Along with the floating-point processor, "this combination brings analysis and simulation capabilities to the engineer's desk," says Dorie.

Saber has enhanced the system with its own direct-memory-access system, which has a data-transfer rate of 20 megabytes/s. Since only information that has been used most recently is kept in random-access memory, other information is moved in and out of mass storage as needed. The IGCS has two independent disk controllers, each on a separate DMA channel with its own disk subsystem. One is allocated to Unix—the Berkeley version has been chosen—the other dedicated to applications. C, Fortran, Pascal, and other program-

ming languages are offered, and so too are many Unix utility packages, like the Programmer's Work Bench.

In essence, the graphics-interface package is based on Siggraph Core primitives and such extensions as a window manager and access to the video lookup tables. The IGCS also supports the international Graphics Kernel System (GKS) standard.

Priced from $40,000 to $70,000, the Saber IGCS work stations will be available in July 1984.

Saber Technology Corp., 2381 Bering Dr., San Jose, Calif. 95131. Phone (408) 945-9600 [Circle 356]

High-speed graphics chip set reduces burden on host microprocessor

Special-purpose microprocessors targeted at high-speed color graphics are beginning to replace the boards full of hardware used in existing systems to produce real-time simulation and animation. The latest comes from Xtar Electronics Inc., a 19-month-old company whose founders gained their experience in the video-arcade-game business.

The company's two-chip Graphics Microprocessor (GMP) and its associated Video Shift Register (VSR) circuit do not achieve the integration level of the recently announced 7300 Color Graphics Controller chip set from NCR Corp., which features more than 100,000 transistors on a single integrated circuit [*Electronics*, April 19, p. 166]. But Xtar officials claim their chip set offers higher system performance.

Xtar engineering vice president Terrence J. Coleman pegs the GMP's speed in drawing lines at 10 times that of the widely used 7220 from Japan's NEC Corp., and says it draws polygons 100 to 1,000 times faster. (NCR puts its chip set's performance at four to five times that of the 7220.)

The two-chip GMP—designated the X1001 and X1002—will integrate about 20,000 transistors on each chip. Honeywell Inc.'s Synertek subsidiary, in Santa Clara, Calif., will fabricate the chips for Xtar, using 3-μm n-channel-MOS technology.

The GMP is a 16-bit processor designed to work in a system with a general-purpose host such as a 68000. (Though any processor may be used, operations are simplified if the host has a 16-bit data bus.) The host communicates with the GMP by loading special graphics instructions into a shared memory, or display list. These instructions are fetched by the GMP, which uses them to draw graphics primitives such as points, lines, and filled polygons into the system frame buffer.

Workhorse. The system's host processor must calculate the vertices of any polygon to be drawn. But in the Xtar system, the GMP relieves the host of the burden of the time-consuming pixel-by-pixel calculations for drawing into the frame buffer.

A key to the GMP speed is its architecture, which allows it to fill in multiple pixels during a single memory cycle. Polygons are drawn one horizontal line segment at a time, starting at the top of a polygon and moving left to right to the bottom. Depending on the frame buffer's size and configuration, up to 256 pixels in a segment can be drawn during one 320-ns cycle, though a 64-pixel maximum will probably be more typical, says Coleman. Segments of 64 or more pixels can be drawn at a rate of 5 ns/pixel, which compares with the 800 ns required to draw a single pixel in 7220-based systems, he points out.

The X1003 VSR circuit will be built for Xtar by an as-yet unspecified supplier using a complementary-MOS gate array with a density of about 1,000 gates. Multiple VSR chips will be used in each system to support the GMP. For example, 16 VSR circuits would be required for a typical system offering a resolution of 1,024 by 1,024 pixels and the ability to display 16 colors simultaneously, Coleman says.

VSR chips serve several functions, including control of the data bus to the frame buffer and the conversion of parallel pixel data from the frame buffer into the serial form needed to drive a color-palette random-access memory. Most systems use a RAM to define the color displayed for each pixel value that comes from the VSR circuits, Coleman says.

Each VSR can control four 16-K-by-4-bit RAMs in the frame buffer. So a typical system offering 1,024-by-1,024-pixel resolution based on 4 bits per pixel would require 16 VSRs handling a frame buffer made of 64 such

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RAMs. Twice the number of VSRs and RAMs would be needed to implement a 1,024-by-1,024-pixel system offering 8 bits of information per pixel. This would raise the number of colors that can be displayed simultaneously to 256, from 16 in the system based on 4 bits/pixel. (Xtar lists the maximum size frame buffer that can be handled by its system at 16 megabytes, which would provide a resolution of 2,048 by 2,048 pixels at an unlikely 32 bits/pixel, or 2^{32} displayable colors.) The VSR contains circuitry that allows dithering, or the filling of polygons with two color patterns to increase the number of visually apparent colors without adding frame memory.

Though the GMP does handle display-list RAM refreshing, the Xtar chip set does not generate cathode-ray-tube synchronization signals or video refresh addresses. This task requires a standard CRT controller chip. The Xtar system's other potential shortcomings include an inability to do real-time shading of polygons for increased picture realism. Unlike the NEC 7220, which includes built-in routines for circle generation, the GMP draws a circle as a many-sided polygon, which is a more software-intensive approach.

Xtar plans to offer samples of the chip set during the third quarter, with production quantities to be available before the year is out. Though volume pricing has not yet been set, samples of the two-chip GMP will sell for about $500. Samples of the VSR will go for $25 each, says Emmett J. (Skip) Powers, Xtar chief executive officer.

Powers expects pricing to follow a typical semiconductor-price-reduction curve, with the two-chip GMP selling for about $45 in quantity after three or four years. The VSR chip will likely sell for about $7.50 by that time. The GMP chips will initially come in 40-pin ceramic dual in-line packages; plastic versions will arrive later. The VSR chip will also be in a 40-pin package, initially Cerdip with plastic versions to come.

Xtar has already sold an exclusive license for use of the chip set in video arcade games. Powers figures the chip set's initial high price will probably limit most use to such high-end systems as computer-aided-design systems and flight simulators. As the price comes down, he expects to see the chips used in add-on graphics systems for personal computers and consumer games.

Xtar Electronics Inc., 2262 Landmeier Rd., Elk Grove Village, Ill. 60007. Phone (312) 364-4111 [Circle 357]

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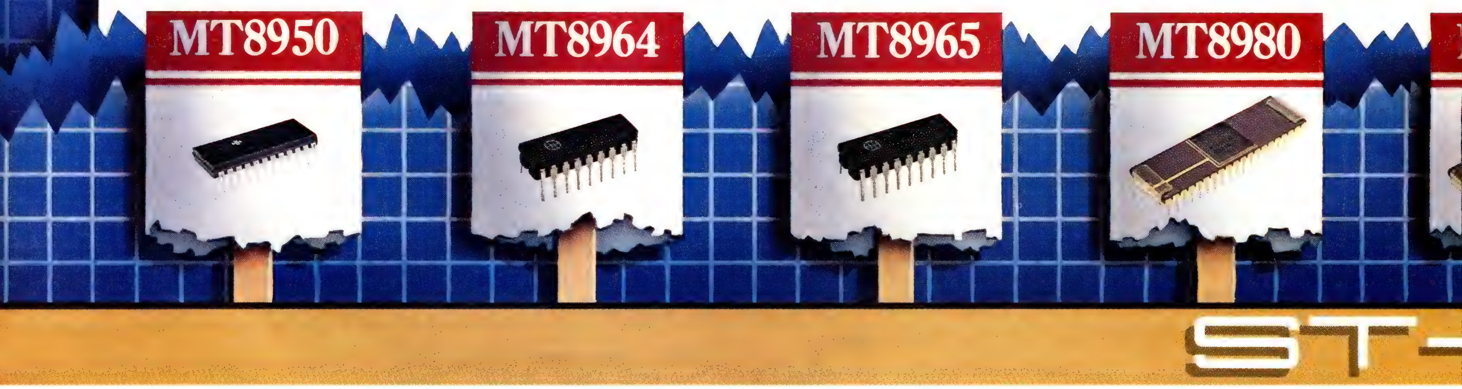

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Instead of using chemical reagents or special reaction chambers to test samples, the A-100 takes conductivity readings to reveal the presence of organic carbon inside the same chamber where compounds are broken down by photoionization. The single-stage process reduces the system's size, so units can be distributed throughout a plant, says Robert M. Brunk, marketing director.

Ultrapure water is often used in various stages of chip fabrication, but as circuit feature sizes shrink, contaminants in water become a potential cause of defects that reduce yields. Today, many advanced semiconductor fabricators produce their own high-purity water through multistage purification systems, which must be monitored.

When organic compounds in the water break down, they oxidize to form carbon dioxide, producing carbonic acid in the solution. This results in detectable conductivity changes, which the unit measures. It can measure the organic compounds that cause these changes in quantities as small as 10 parts in 10^9. Analysis cycles take 3 to 5 min.

Breakthrough. The microprocessor-based A-100 system is a breakthrough in the packaging and pricing of a total organic-carbon analyzer for the IC industry, says the firm. The A-100 weighs a total of 12 lbs and breaks down and measures total organic-carbon levels in an enclosure about the size of a household fuse box. An automatic valve traps water in the test chamber, and measurement data is stored in the controller's memory.

Laboratory-targeted water analyzers are typically much larger than the Anatel system. Many cannot be connected directly to water lines and weigh as much as 300 lbs in packages the size of a footlocker.

The system is split into two components: a controlling unit and a sensor. Both units, which are connected by an RS-232-C interface, contain Z8 microprocessors. In addition, the controller has a math coprocessor and memory chips.

The control unit—in a splash-proof panel-mount enclosure—features touch-sensitive switches, light-emitting-diode trend-indicator arrows, a four-quadrant bar graph, and alarm. A hard-copy output device and an RS-232-C port are optional.

The system operates from a power supply of 115 V ac at 60 Hz or 230 V ac at 50 Hz. It can operate in temperatures ranging from 15° to 40°C (ambient) and with water pressures up to 100 lbs/in^2.

In single quantities, the A-100 costs $9,000. Initial deliveries are now beginning; high-volume deliveries will begin in mid-summer.

Anatel Instrument Corp., 2200 Central Ave., Suite F, Boulder, Colo. 80301. Phone (303) 442-5533 [Circle 358]

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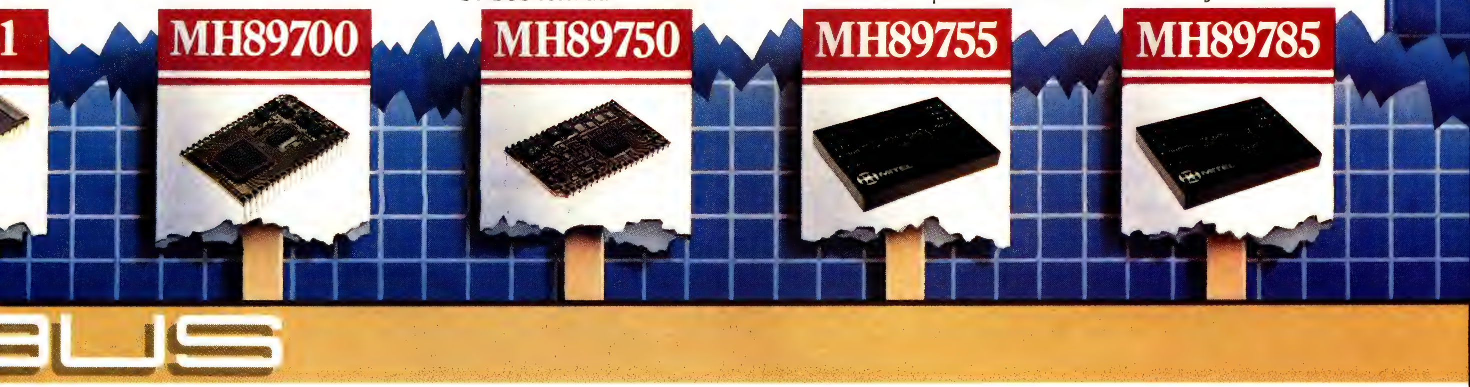

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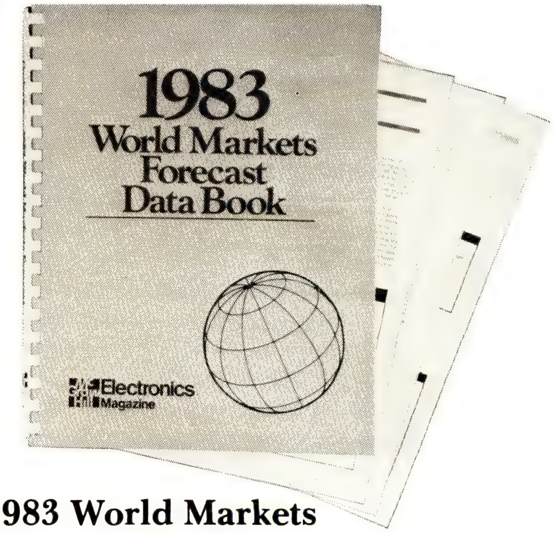

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The system handles multiuser applications for distributed computing, data processing, engineering work stations, and office automation. Capable of supporting up to 32 interactive users, the Harris 60 performs decision-support, computer-aided-design, and software-development applications simultaneously.

The basic system includes a two-board central processing unit; a communications controller; an 80-megabyte, 8-in. Winchester disk drive; a 23-megabyte, ¼-in. cartridge-tape drive; an operator communications terminal as a systems console; and the virtual operating system. A cache option in the Harris 60 cuts memory-access time and typically improves performance by 20%.

First shipments of the Harris 60 are scheduled for June. The system is priced at $69,500.

Harris Corporation, Computer Systems division, 2101 W. Cypress Creek Rd., Ft. Lauderdale, Fla. 33309. Phone (305) 974-1700 [Circle reader service number 361]

Trio of color monitors offers choice for small computers

Intended for personal and small business computers, the model DT-S101 color video monitor displays 40 characters by 25 lines of text. The monitor features a switch that eliminates chroma to provide white letters on a black background.

A companion red-green-blue display, the DT-H103, can reverse background color and characters when a button is pushed. Its resolution is 640 by 480 picture elements.

A desktop teletext display system, the DT-M140, features a cathode-ray tube with composite RGB. The square-cornered, 14-in. diagonal CRT produces an 80-character by 25-line display.

Available now, the DT-S101 is priced at $330, and the DT-H103 goes for $753.

Panasonic, 1 Panasonic Way, Secaucus, N.J. 07094. Phone (201) 348-7183. [Circle 364]

Head-cleaning software gives directions on screen

A floppy disk for head cleaning also provides cleaning instructions on screen for the International Business Machines Personal Computer and the Apple IIe/II Plus, and another version is designed for the Atari 800 and 800XL and the Commodore 64.

When loaded in a computer and booted, the disk gives instructions on the screen for selecting which disk drive is to be cleaned and how to prepare a separate cleaning disk for placement into the disk drive. The program runs the read/write heads on an unused band of the cleaning disk for 30 seconds, shuts off the disk drive, and keeps track of how many cleaning cycles are left on the disk.

Available now, a kit that includes two disks, a reusable disk jacket, head-cleaning spray, and instructions is priced at $39.95

Nortronics Company Inc., 8101 Tenth Ave., North Minneapolis, Minn. 55427. Phone (612) 540-8674 [Circle 368]

Fault-tolerant minicomputer uses 68010 microprocessor

Designed for fault-tolerant operation, the Parallel 300 minicomputer has a redundant architecture with all vital components—including processors, power supplies and battery-backup systems, disk drives, and disk controllers—duplicated. By simply removing thumbscrews, nontechnical people can replace any faulty element. Until this is done, backup hardware keeps the system running.

The system's coupled pair of parallel processing units uses Motorola's 68010 virtual-memory microprocessors running at 10 MHz without wait states. There are two Winchester disk drives and disk controllers, and all data is written on both disks.

Priced at $75,000 for the end user, production versions of the Parallel 300 will be available in late May.

Parallel Computers, 3004 Mission St., Santa Cruz, Calif. 95060. Phone (408) 429-1338 [Circle 365]

Graphics unit for IBM PCs generates 35-mm slides

A business graphics system called Samurai, which can be plugged into an International Business Machines Corp. Personal Computer, produces 35-mm slides with a resolution exceeding 4,000 lines. The system consists of a self-contained 35-mm film recorder weighing 50 lbs., a single graphics processor board that plugs

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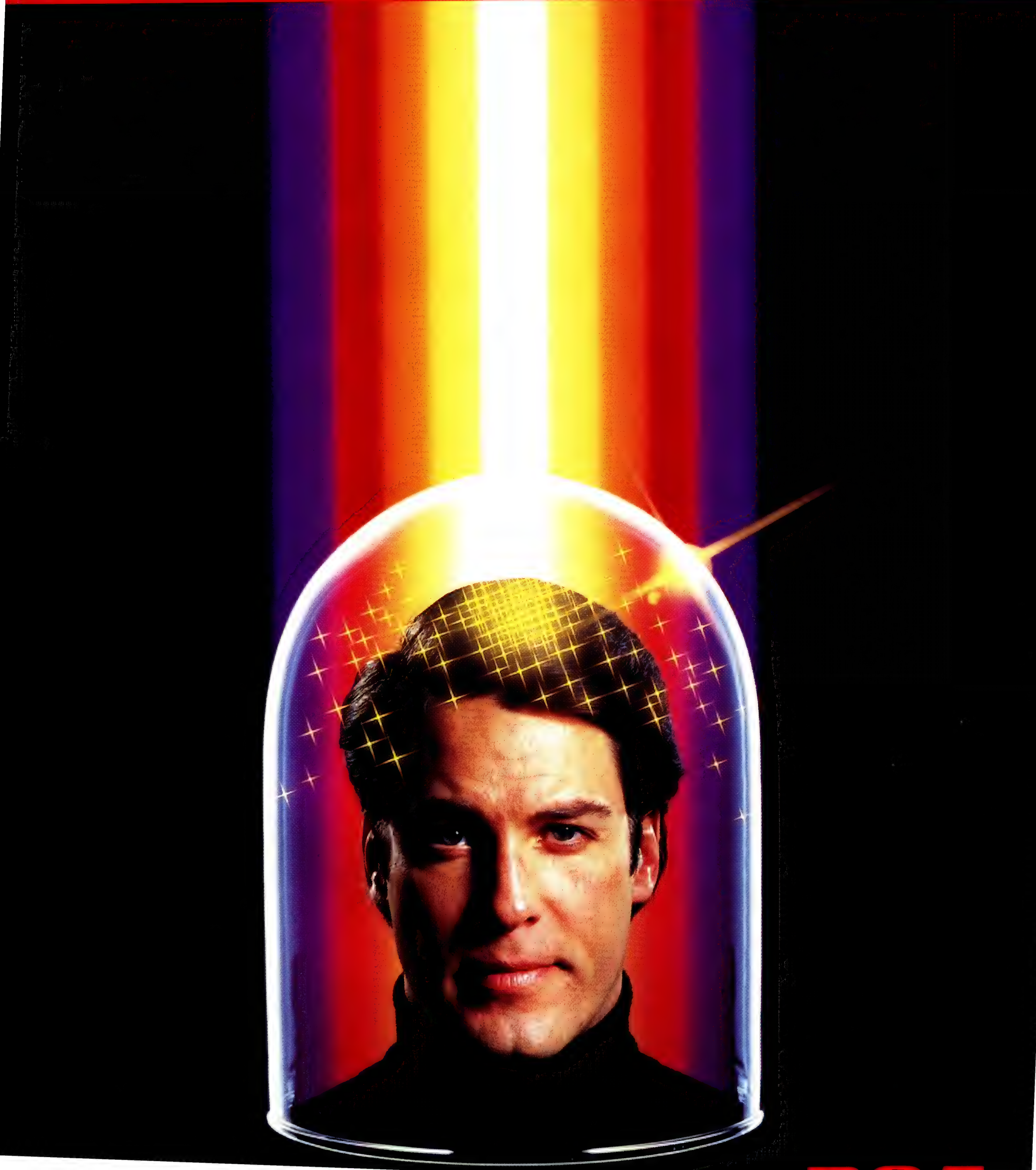

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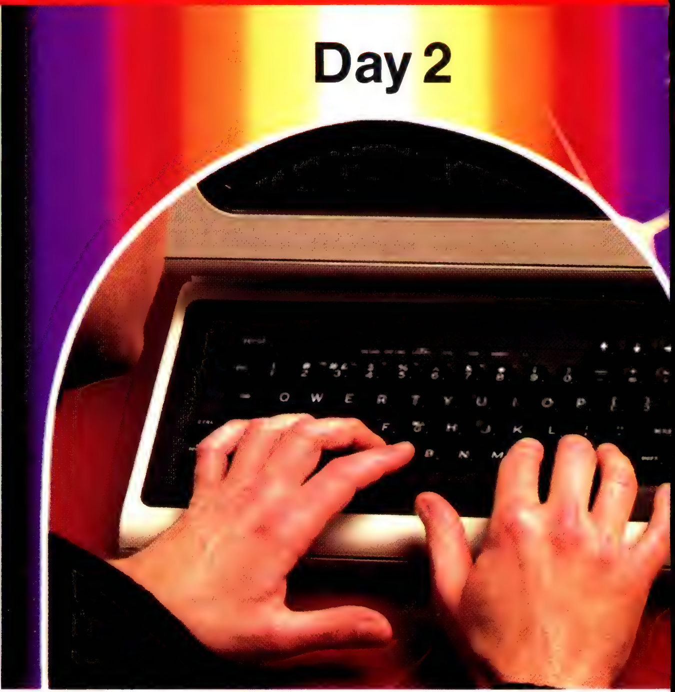

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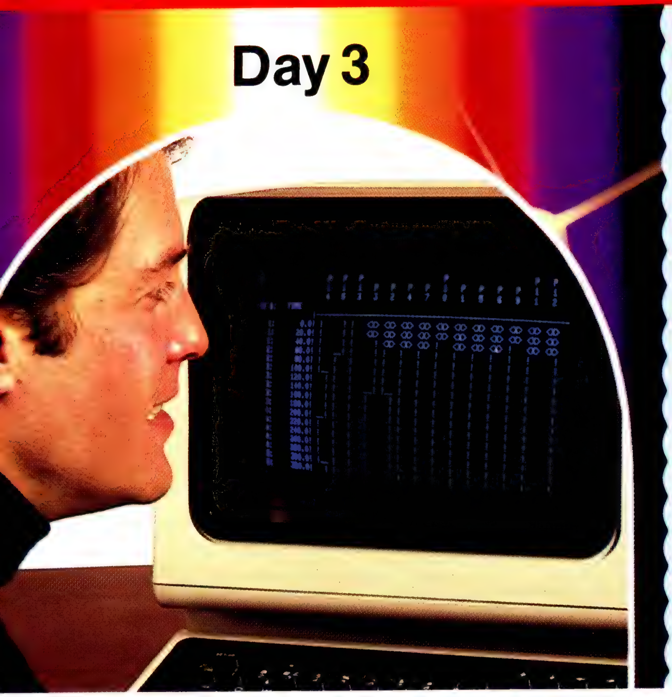
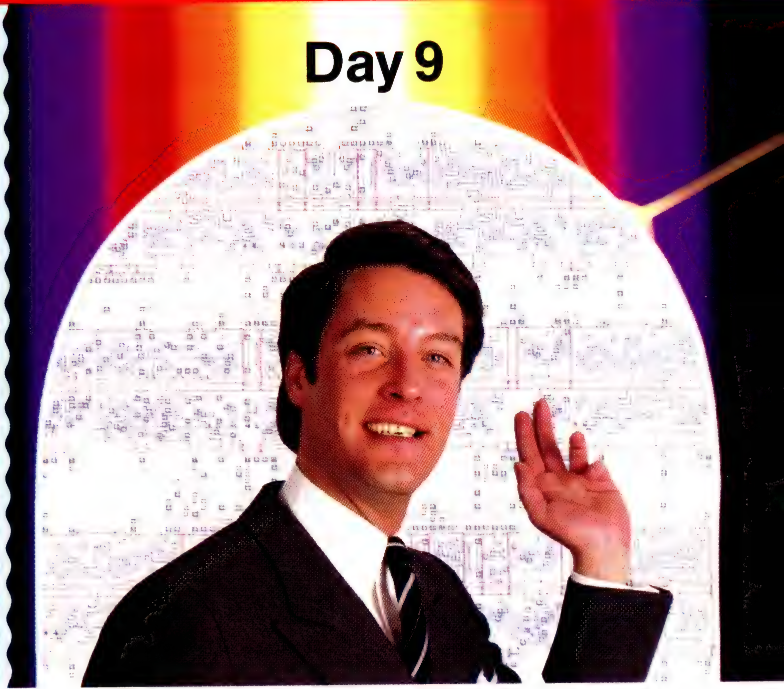


Your completed design may be tested and verified using programs such as this wave form analysis. From your own location you complete the documentation package and return your design to RCA for tooling and fabrication of prototype.



Typically by the ninth day, you can show your completed circuit design to your management. RCA has already audited the design package, placed, routed and optimized for bondability, verified critical path timing specifications and provided you with a layout and specifications for final approval.

from 3ns to 20ns and up to 4500 gates.

Of course, all our circuits are in CMOS, which was invented by RCA.

Second sources second-to-none.

Second sourcing is a very touchy subject for most semicustom suppliers. RCA offers one of the few "true" second sourcing agreements in the industry. RCA 50,000 Series is alternate sourced by LSI Logic using direct transfer of custom mask tooling and test programs between both suppliers. So there's no need to redesign on another system to have a second source. In standard cells, RCA has recently completed a joint development agreement with Silicon Systems to create a new library of digital and analog standard cells.

Remember too, when you're linked to an establishment like RCA, second sourcing is not as critical as when dealing with less established suppliers. Many satisfied customers currently use RCA as a sole source.

Guaranteed success says it all.

We believe RCA semicustom systems and software are unsurpassed in the industry. First time success is virtually assured. RCA takes responsibility for supplying product that meets the simulation signed off by RCA and the customer. And we guarantee that if reiteration is required due to an RCA error, RCA foots the bill.

Strategic partnering: to have and to hold.

RCA has made a commitment to be a leader in CMOS semicustom. Semicustom is our priority, commanding resources, research and responsiveness to your needs. Where we share mutual goals for growth, RCA can introduce you to our strategic partnering capability, working side by side to match our resources to your needs and future plans.

Megachange at RCA.

Semicustom Simplified is just one example of the big changes taking place at RCA. Our new Total CMOS Logic Service offers you one-stop shopping for QMOS high-speed CMOS logic, memories, micros, peripherals and High Rel components. All with RCA quality, RCA reliability, and RCA competitive prices.

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But throughput isn't everything; on a per-chip basis, you'll find Ando testers can actually **lower** your charges for testing and development. Here are some of the reasons:

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into the PC expansion slot and a shielded cable.

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Selling for under $10,000, the system will be available in August.

Image Resource Corp., 733 Lakefield Rd., Westlake Village, Calif. 91361. Phone (805) 496-3317 [Circle 366]

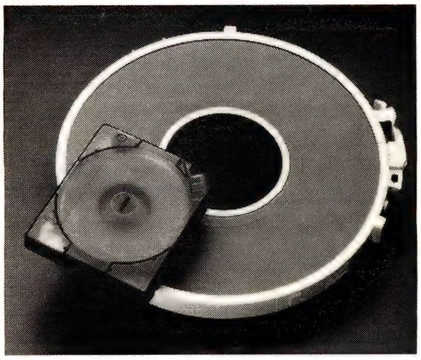
Cartridge tape drive provides faster data access than reels

Cartridges are in and reels are out in the IBM 3480 line of magnetic tape drives. The rectangular cartridge is about one fourth the size of a standard 10.5-in. reel, but stores up to 20% more data—a total of 200 million characters.

The 4-by-5-in. cartridge is inserted into a slot in the drive. Two of them are contained in a cabinet that is about the size and shape of a two-drawer office file. Information from a central processor can be transferred to the tape drives or retrieved from them at rates of up to 3 million characters per second—more than twice the rate at which current IBM tape drives read and write data.

The price of a typical IBM 3480 magnetic tape subsystem, consisting of one controller and eight drives, is $237,910; the equipment will be available in the first quarter of 1985.

International Business Machines Corp., Information Systems Group, 900 King St., Rye Brook, N. Y. 10573. Phone (914) 934-4488 [Circle 362]



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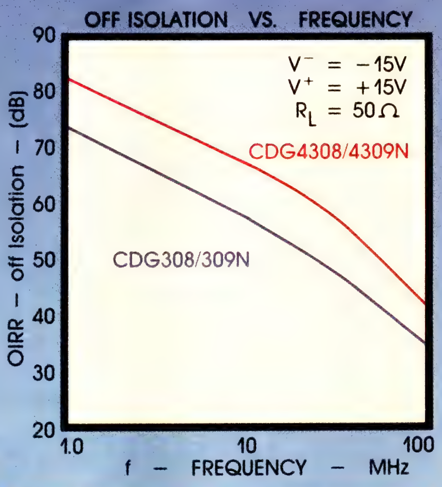

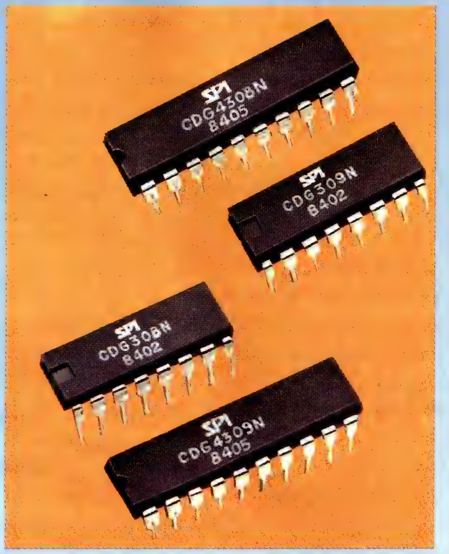

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Data Acquisition

12-bit hybrid a-d converter runs at 500 kHz

The ADC-00403, a 12-bit successive-approximation analog-to-digital hybrid converter in a 32-pin hermetic dual in-line package, is designed for military and industrial data-conversion requirements. It is a pin-for-pin replacement for ADC85 and ADC87 types, but at 2 μs, it operates at higher speeds.

The converter's digital outputs include both serial and parallel output data, as well as conversion status line. Output coding for unipolar input operation is complementary binary; for bipolar input operation, complementary-offset binary or 2's complement formats are used.

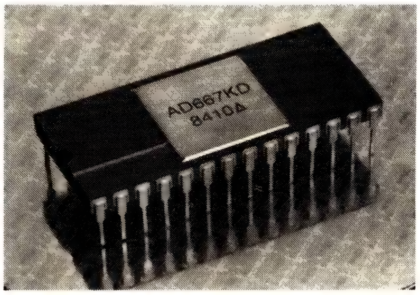
Other features include a precision internal reference and six-pin programmable unipolar and bipolar input-voltage ranges. Linearity, gain, and offset errors are within 0.1% of full scale and 0.05% of full scale, respectively.

Priced at $169 for the 0°-to-70°C model and $219 for the –55°-to-+125°C model, the ADC-00403 is said to cost less than available hermetically sealed military-temperature-range units. Small quantities are available within eight weeks.

ILC Data Device Corp., 105 Wilbur Pl., Bohemia, N. Y. 11716. Phone (516) 567-5600
[Circle reader service number 381]

Digital-to-analog converter has double-buffered interface

A monolithic 12-bit digital-to-analog converter provides a universal microprocessor interface, maintains high accuracy over temperature changes, and includes an on-chip buffer amplifier that produces an output voltage to settle within ½ least-significant bit in 3 μs maximum.



The AD667's double-buffered microprocessor interface is easy to use. The first register bank consists of three parallel 4-bit latches that can be enabled separately or together to facilitate loading from a bus of any size in 4-, 8-, or 12-bit words. Once assembled, the word is transferred into a 12-bit-wide latch that drives the d-a converter.

The analog output features nonlinearity specified at within ½ LSB on K and B grades. All versions are guaranteed to be monotonic over their temperature ranges.

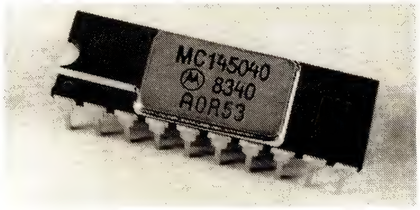
Available from stock, the product ranges in price from $9.90 for orders of 1,000 pieces for the JN grade to $80 per unit for 100-piece orders of the leadless chip-carrier versions.

Analog Devices, Route 1 Industrial Park, P. O. Box 280, Norwood, Mass. 02062. Phone (617) 935-5565 [Circle 382]

Converter runs on 4 to 6 V for use with MOS systems

The MC145040 analog-to-digital converter offers features such as a supply-voltage range of 4.0 V to 6.0 V for operation in n-channel and complementary-MOS systems, an operating range of –55° to 125°C, and a conversion rate of 16 μs for the standard part.

The MC145041 offers an on-chip oscillator that allows integration with low-cost microcontrollers that do not put out a clock signal. The two 8-bit a-d converters have serial interface ports and are compatible with Microwire interfaces, among others.



Available now, samples of the MC145040 cost $2.89 each in orders of 100 or more. MC145041 samples cost an additional 10¢ each.

Motorola Inc., MOS Integrated Circuits Group, 3501 Ed Bluestein Blvd., Austin, Texas 78721. Phone (512) 928-6880 [Circle 383]

Six of unit's multiplexed inputs handle digital or analog signals

The ADC0829, a successive-approximation analog-to-digital converter designed for industrial and consumer markets, has an 11-channel multiplexer that lets 6 channels be used as digital and analog inputs.

The 8-bit monolithic complementary-MOS device contains channel selection, conversion contol, and bus-interface logic. It is designed to operate from a microprocessor data bus using a 5-V supply and features a 0-to-5-V analog input range and a temperature range of –40° to +85°C.

Packaged in a molded 28-pin dual in-line package, the version with ½ least-significant-bit total unadjusted error is available now and in lots of more than 100 pieces sells for $6.95. The 1-LSB version is also available now for $3.95 in lots of 100.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 721-5000 [Circle 384]

Frequency-to-voltage module has one of five input ranges

The model PRA1 frequency-to-analog converter is a plug-in module that transforms the frequency signal from a machine-mounted sensor into analog voltage and current signals proportional to the frequency. The converter's output then drives such instruments as chart recorders or a speed-control signal.

The unit is available in five frequency ranges from 30 Hz to 10 kHz. Input circuit configuration and current-range output is switch-selectable. Converters are available for ei-

This new FET solid state relay can turn on or off in 500 microseconds.

Our new C46F (AC output) and C47F (DC output) relays feature a 500 microsecond turn on/off time. But they also use power FET technology to eliminate the bipolar offset voltages normally associated with solid state relay outputs.

Add these qualities to the renowned reliability of FET SSR's, and the fact that they are "bounce free," and you now have ideal solid state replacements for reed relays.

Such applications could include low level switching, for general purpose analog and transducer signal switching, telecommunications, load control from microcomputer I/O ports, and data couplers.

Both relays are, of course, pin compatible with DIP reeds.

Optical coupling from input to output typically provides 1000 volt dielectric isolation. Therefore input logic circuits are protected from deadly transients and surges.

There is also buffering so the relay can be driven by TTL logic.

Internally, hybrid microcircuit techniques are incorporated into a patented lead frame design for low cost as well as superior physical integrity.

The complete assembly is then molded in a standard 14 pin TO-116 DIP package.

The custom microcircuit design features a constant current input which means that the current required to turn on these devices remains at a nominal 12 milliamp level at any input voltage from 3.8 VDC to 32 VDC. No external current limiting is needed which allows for high PCB packaging density.

Outputs are rated to 400 volts AC or DC, with load current switching capability up to 400 milliamps, and on-state resistance as low as 7 ohms.

For complete technical information on the C46F and C47F, call or write. You'll see how and why it makes perfect sense to finally replace all those reed relays for the very last time.

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Circle 201 on reader service card

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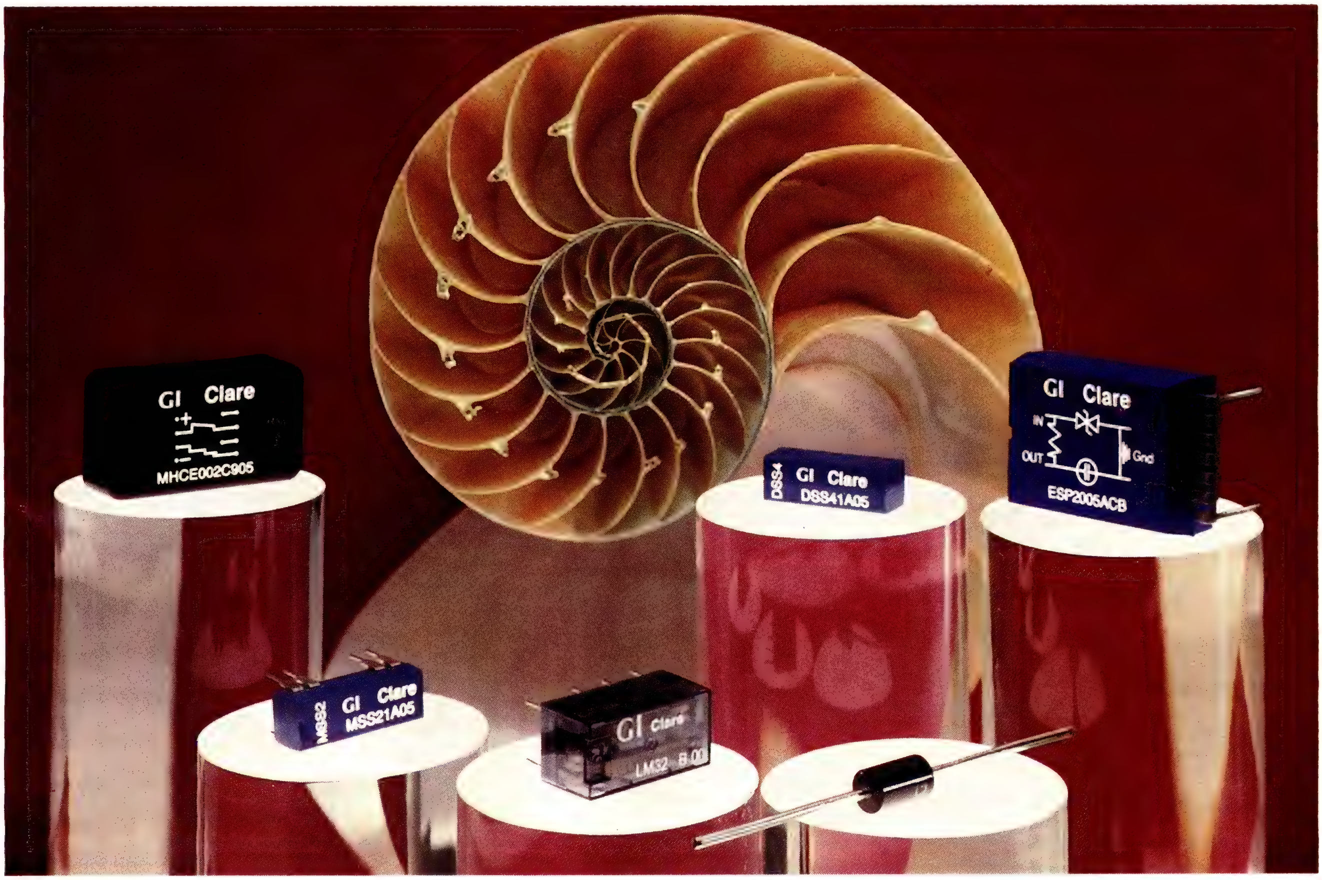

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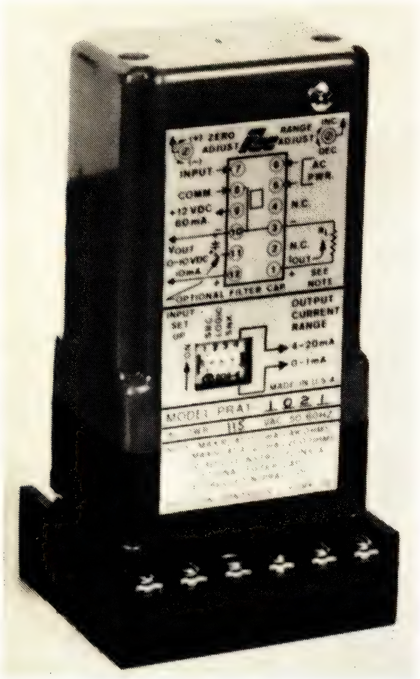

ther 115 or 230 V ac power.

Priced at $98, the product is available in two weeks.

Red Lion Controls, Willow Springs Circle, RD 5, York, Pa. 17402. Phone (717) 767-6511 [Circle 385]

Digital-to-synchro converter puts out as much as 25 VA

A series of digital-to-synchro converters has 14-, 12-, or 10-bit resolutions and can drive torque receivers with an accuracy within 10 min of arc. The devices provide up to 25 VA.

The converter measures 4.5 in. by 9.25 in. and will accept a 14-bit natural binary angle and convert it into three-wire synchro or four-wire resolver signals. The output is protected against short circuits, thermal overloading, and transients.

The unit needs a 26-V reference and two supply voltages: ±15 V at 65 mA plus the load current, and 5 V at 100 mA. Operating-temperature ranges are 0° to 70°C or –55° to 85°C.

Priced under $895 each, the product can be delivered in four weeks.

Computer Conversions Corp., 6 Dunton Ct., East Northport, N. Y. 11731. Phone (516) 261-3300 [Circle 387]

A New Generation of Subminiature DIP Switchers From Clare

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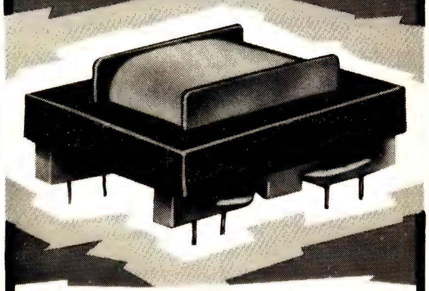

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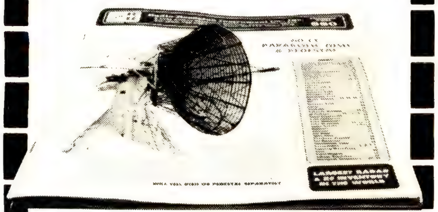

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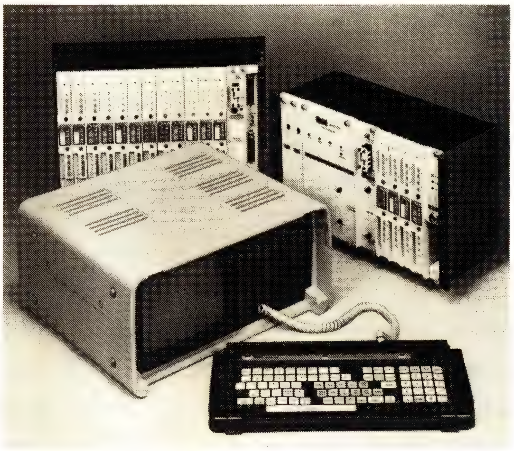

The 620-10 is a single-module processor that increases the reliability of relay applications. Combining data handling with relay ladder logic, the 620-15 processor is a smart single-module unit, while the 620-20 processor is a fast multimodal one. As for the 620-30 processor, which was designed for high-speed control applications, it can do what the others can and also has an advanced instruction set and additional memory.

Intercomponent communications can be achieved through one or more of the 620's network capabilities. A stand-alone industrially hardened microcomputer performs a range of monitoring, reporting, and communications tasks. Self-diagnostics are incorporated to simplify maintenance.

Pricing for a typical IPC 620, which is available immediately, starts at $4,000.

Honeywell Inc., Honeywell Plaza, Minneapolis, Minn. 55408. Phone (800) 328-5111 [Circle reader service number 371]

Series of magnetic-latch relays has contact ratings of 5, 10 A

The series 68RM, a low-cost magnetic-latching relay, comes in single-pole, double-throw; double-pole, double-throw; and triple-pole, double-throw configurations, with dc single- or double-wound or ac coils and contact ratings of 5 and 10 A. The relays' features include low power consumption, continuous operation, and TTL compatibility.

The relays' energy efficiency derives from its ability to remain latched indefinitely in an open or closed state, without additional current, until it is reenergized to switch contacts. Its latching function lets the relay be used as a time-delay switch.

The 68RM costs $8 a unit for quantities of 1,000; for standard models, delivery is from stock.

Sigma Instruments Inc., 170 Pearl St., Braintree, Mass. 02184. Phone (617) 843-5000 [Circle 372]

Transducer measures forces as low as mosquito footsteps

The model 406 transducer system can measure forces as low as 1 μg, such as snowflakes, mosquito footsteps, and colliding microscopic particles. The unit can measure up to 50 mg full scale, and its 100-Hz, 3-dB down-frequency response makes possible a critically damped step response of 5 ms.

The system's design is based on a variable displacement capacitor whose plates are formed from an

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etched, cantilevered, quartz beam. An integral reference element allows operation without expensive laboratory techniques.

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Cambridge Technology Inc., 2464 Massachusetts Ave., Cambridge, Mass. 02140
[Circle 374]

Control processor handles distributed data acquisition

Designed for remote-data acquisition, an industrial-control processor is suited to applications involving widely distributed networks and unattended operation. Based on the company's single-chip T11 processor, CMR21 is targeted for original-equipment manufacturers and large-volume end users.

It features industrial packaging, read-only-memory-based firmware, built-in diagnostics, and base-level PDP-11 software. CMR21 can be used as a stand-alone device or linked in networks through public or private telecommunications lines.

Available now, the controller is priced from $3,900.

Digital Equipment Corp., 129 Parker St., Maynard, Mass. 01754 [Circle 375]

Square-matrix unit prints custom-designed labels

The model 8625 square-matrix flexible-format printer allows users to design labels containing graphics information and bar codes of varying heights and densities, to define the bar code's location on labels, and to

No Shift. Sure Lock.

Symbex factory produced IDC Cable Assemblies eliminate problems associated with "crimped-on" IDC assemblies.

ELIMINATE CABLE/CONNECTOR SHIFT.

The problem of cable/connector shift can cause short or long term unreliability of IDC joints.

Misalignment of components during the crimping process can produce assemblies with intermittencies, line by line impedance variations or a total lack of continuity.

The Symbex "molded-in" process of IDC assembly eliminates those concerns. Contact and conductor "shift" is impossible. When the IDC's are made, perfect alignment means no conductors are cut. Clearly a better method that is uniquely reliable.

IDC LOCKED SOLID.

The problem of excessive or repeated strain on the cable at the connector interface can cause long term unreliability of the IDC joints with typical crimped-on IDC's.

Mechanical covers (primary or secondary) are just that, mechanically attached. They can unlock and do become loose.

The Symbex "molded-in" process of IDC provides a sure lock and eliminates those concerns. The entire connector is formed around the conductors and contacts within an injection mold – creating the one piece "molded-in" result. Strain relief is integral and gas-tight IDC's are vibration free. *Uniquely superior to all other methods.*

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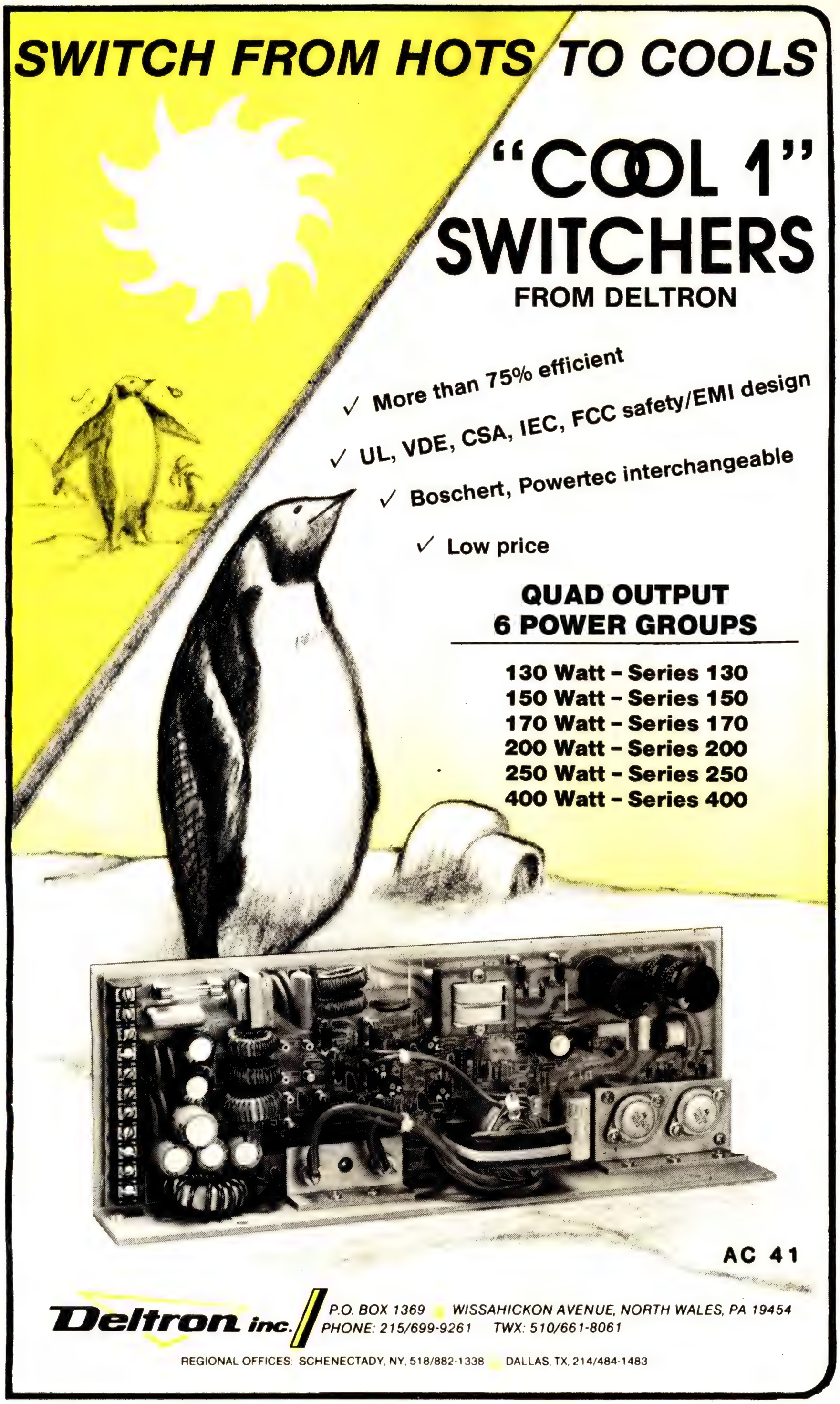

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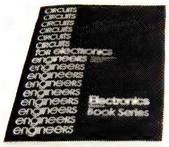
Circle 208 on reader service card



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The 8625's bar-code symbologies include Code 39, Code 93, Code 11, Codabar, and UPC/EAN. Three graphics fonts printed in any magnification are available, and text can be printed in four directions. Plug-compatible with most minicomputers, the system can define unique characters for special graphics or logos.

At a price of $2,995, the printer is available from stock.

Intermec Corp., 4405 Russell Rd., Lynnwood, Wash. 98046-9702. Phone (206) 743-7036 [Circle 373]

Miniature pressure probes are as thin as 0.020 in.

The EPI series of transducer probes measure static and dynamic pressure where small size and difficulty of access are major problems. Its uses include wind-tunnel and flight tests, as well as bioengineering research.

The EPI series uses the company's EPI-080 pressure transducer, which can measure pressures from 0-2 to 0-500 lb/in^2 with outputs as high as 125 mV and resonant frequencies to 420 kHz. Barrel-shaped and threaded probes can be had in custom diameters and lengths. Paddle-shaped units as thin as 0.020 in. are available for surface measurements.

In quantities of one to nine, the pressure transducer probes cost $360 and are available now.

Entran Devices Inc., 10 Washington Ave., Fairfield, N. J. 07006. Phone (201) 227-1002 [Circle 377]

M-5e

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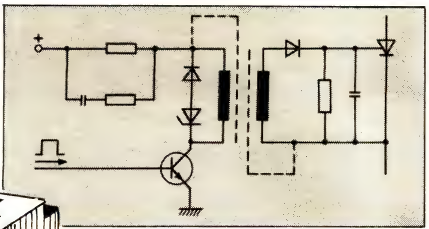
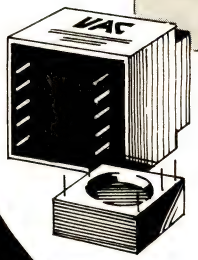
for SCR-Firing





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Circle 78 on reader service card

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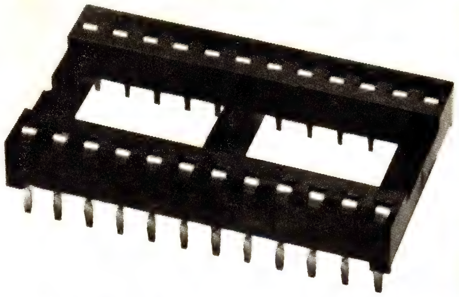

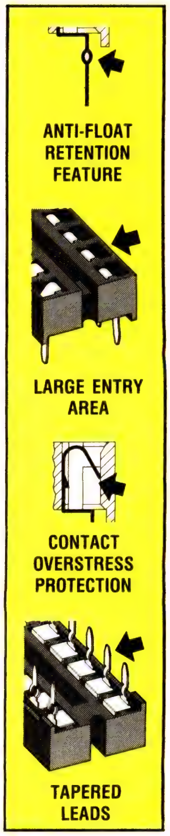

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Called the Welcon Series 801, this new line of DIP production sockets features a single face-wipe contact. This socket provides many outstanding advantages at a very competitive price! A low contact resistance coupled with a high retention force. A wide target area and chamfered cavity for easy insertion of IC devices. An anti-float feature to hold the socket in place during the soldering process. Tin-plated, phosphor bronze contacts. A very low profile . . . only .175″ off the p.c. board. Machine insertable. Available in 8- to 40-leads.

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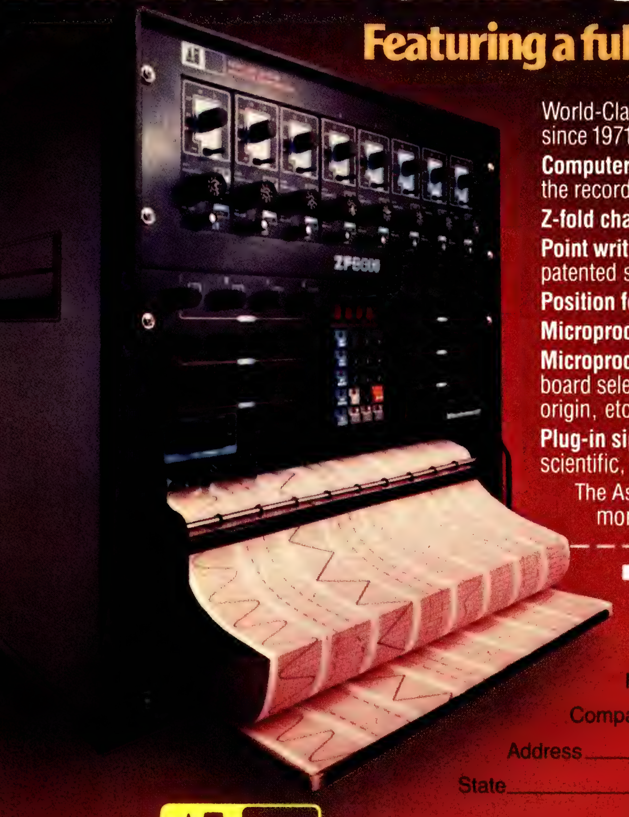

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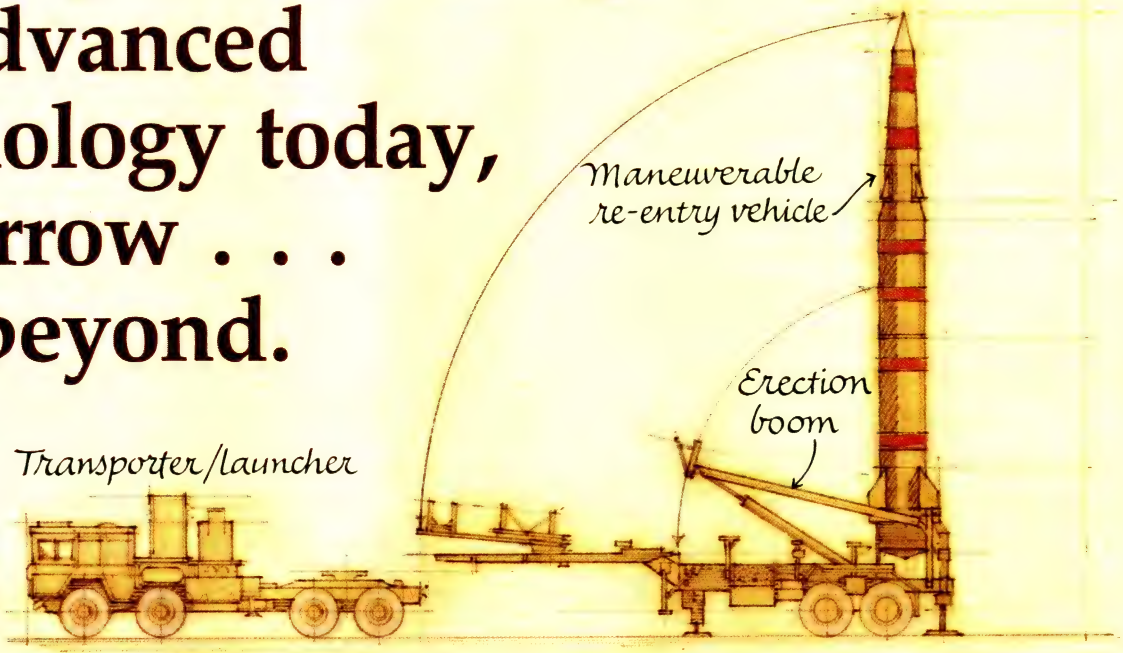

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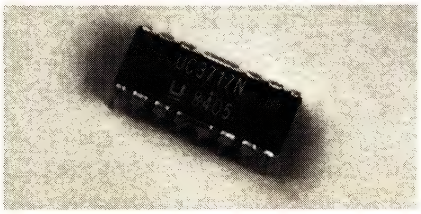
Components

Schottky diodes let motor IC recover quickly

Designed for bipolar stepper-motor controls, the UC3717 integrated circuit consists of a logic input compatible with low-power Schottky TTL, a current sensor, and an output stage with built-in Schottky protection diodes. Selection of the Schottky diodes instead of p-n junction diodes was to achieve faster recovery times and lower forward voltage drops, thus reducing electromagnetic interference and power dissipation.



The UC3717, pin-for-pin compatible with the RIFA PBL 3717, is a constant-current chopper drive designed for high-performance even with unstabilized motor-supply voltages of 10 to 45 V and output current from 10 mA to 1,000 mA. The current levels can be selected in steps or varied continuously. In addition, the IC can operate in full- or half-step modes, and a built-in time delay prevents short circuits in the output stage during phase shift.

The 100-piece price is $4.03, and delivery takes six weeks.

Unitrode Integrated Circuits, 7 Continental Blvd., Merrimack, N. H. 03054. Phone (603) 424-2410 [Circle 421]

Negative regulator sinks 3 A over wide voltage range

A three-terminal, adjustable negative-voltage regulator, the LM133, can sink in excess of 3 A over a range of –1.2 V to –32 V. When a positive 3-A power supply is required, another series of adjustable positive 3-A regulators can be used.

The LM133 series features internal current limiting and thermal shutdown, which protects the regulator when the output is short-circuited or when the device overheats. Two inexpensive resistors and one capacitor are the only external components required to set the output voltage. The company provides 100% thermal limit burn-in testing.

Available now in TO-3 and TO-220 packages, the standard part of the series, the LM333, sells for $5.90 and $3.45, respectively.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 721-5000 [Circle 422]

Operational amplifier slews at 500 μV/μs

The model 1815 operational amplifier, which slews at 500 μV/μs, is designed for video amplifiers, deflection amplifiers for cathode-ray-tube terminals, analog-to-digital input amplifiers, digital-to-analog output amplifiers, and similar applications. The unit's small-signal bandwidth is 70 MHz, and its full-power bandwidth is 8 MHz. With 100-mA output current, the 1815 settles to 0.1% in 100 ns.

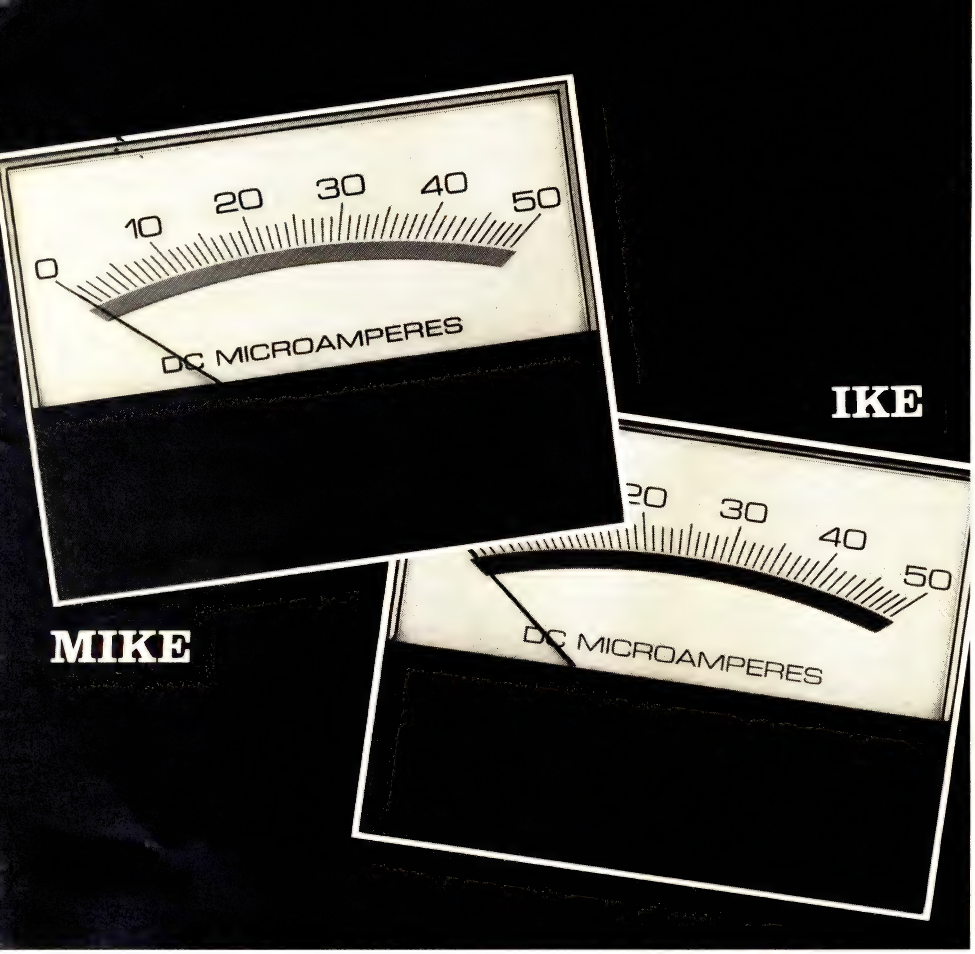
Priced at $77 for 100-piece orders, the 1815 can be delivered in a week.

Dynamic Measurements Corp., 8 Lowell Ave., Winchester, Mass. 01890. Phone (617) 729-7870 [Circle 423]

Gain-bandwidth product is 1 GHz in wideband op amp

The AM-1435 wideband operational amplifier can be used for radar and sonar processing, video instrumentation, and ultrafast data-acquisition. It has an open-loop gain of 100 dB, a flat frequency response beyond 10 kHz, and a 6-dB/octave roll-off to beyond 100 MHz. Gain-bandwidth product is typically 1 GHz, and slew rate is 300 V/μs.

Its dc characteristics include 1-MΩ input impedance, an initial offset



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Circle 212 on reader service card

voltage within 2 mV, and an input-offset-voltage drift within 5 μV/°C. Minimum common-mode rejection ratio is about 80 dB, and full power frequency is a minimum of 8 MHz. The output-voltage swing is within 5 V minimum at a 10-mA load current, and the AM1435 is stable with capacitive loads up to 1,000 pF.

The AM-1435MC, with an operating range of 0°C to 70°C, is priced at $68. The AM-1435MM, with an operating range of -55° to +125°C, is priced at $102. Both can be delivered within six weeks.

Datel, 11 Cabot Blvd., Mansfield, Mass. 02048. Phone (617) 339-9341 [Circle 424]

Sealed rotary switches have high contact stability

The DR series of binary rotary switches are 0.394 by .0232 in. high and are sealed to prevent flux and other impurities from reaching the contact mechanism during washing. The switches are available in real- or complement-coded models and with screwdriver or shaft-type actuation.

High contact stability is further ensured by gold-plated contacts. The switches' formed terminal design prevents slippage during wave soldering. The terminals are adaptable to dual-in-line-package sockets.

The switches are priced at $1.30 for 100-piece quantities; delivery takes six to eight weeks.

NKK Switches, 14415 N. Scottsdale Rd., Suite 600, Scottsdale, Ariz. 85260. Phone (602) 991-0942 [Circle 426]

Symbolic keyboard speeds retrieval from image disks

A symbolic keyboard for the company's system 6000 work station features cartoon-like characters and can be used in automotive, retail, aviation, and aerospace applications. The keyboard speeds access to and retrieval of information, such as parts catalogs and maintenance manuals, from image disks that can hold up to 6,000 pages of text and reduced graphics, as well as 4 million characters of digital data.

During a keyword search, the user selects attributes from a dictionary that describes the item and instructs the work station to search for pages that match. Under the system's hierarchical method, the user selects from a top-level menu, at which point he is given additional choices representing subsections of the original selection. The browse indexing scheme is implemented using next-page and previous-page symbols on the keyboard.

The system is priced at $3,350 per work station. A pilot operation can be delivered in 90 days.

Mnemos Sales and Customer Service Inc., 3131 Princeton Pike, Lawrenceville, N. J. 08648. Phone (609) 896-3450 [Circle 425]

Umbrella-style buttons have 25-kV isolation from static

Available in standard, encoded, and indicator-only versions, umbrella-style buttons isolate against a 25-kv electrostatic discharge.

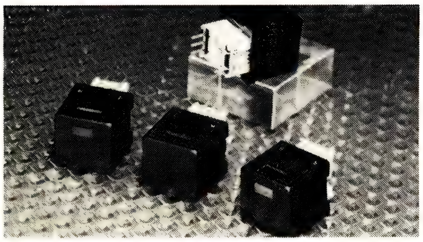
For standard switching, the umbrella button is used with an MML21 electronic control switch. The encoding-switch version provides up to 16 different binary-coded-decimal outputs. Coding is done through cams on the button.

When used as an indicator only, the umbrella button is combined with an MML41 indicator unit. Versions are available with red, yellow, or green light-emitting diodes; for incandescent displays, more colors are offered.

Available now, the button sells for about $1.50 in quantity.

Micro Switch, 11 W. Spring St., Freeport, Ill. 61032. Phone (815) 235-6600

[Circle 427]



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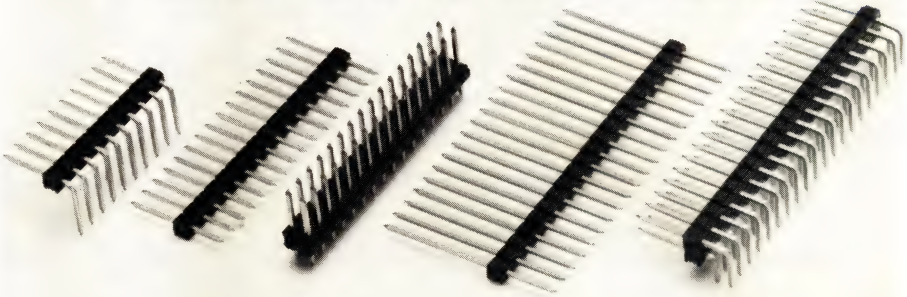

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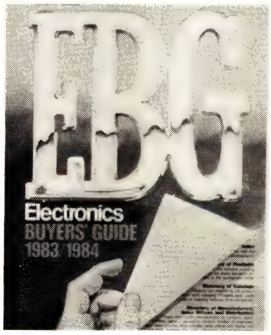

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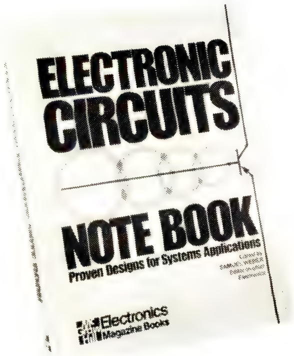

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Power supplies

Switcher series ranges up to 60 V and 300 A

Available in eight models ranging up to 60 V and 300 A, the LT series of power supplies is well suited for laboratory, burn-in test, systems, and various other applications.

The series offers line regulation to within 0.02% plus 2 mV for variations from 187 to 242 V ac. Load regulation is ±0.02% plus 2 mV on models LT-801, 802, 821, and 822, and ±0.02% plus 4 mV on the 803, 804, 823, and 824. All models in the series have a ripple specification of 15 mV root mean square, 100 mV peak-to-peak. Efficiency is rated at 70% at maximum output voltage for the 820 series, and 65% for the 800 series.

Also featured are built-in over-voltage protection and dual digital-meter readout for voltage and current. All models are compatible with the company's IEEE-488-programmable power system.

Available immediately, the LT-820 series is priced at $2,900 and the LT-800 series at $1,650.

Lambda Electronics, 515 Broad Hollow Rd., Melville, N. Y. 11747. Phone (516) 694-4200
[Circle reader service number 401]

Modular switchers meet international noise, safety rules

The compact 25-W 930 series of switching power supplies is guaranteed to have 80% minimum efficiency and comes in three models with outputs of 5 V at 5 A, 12 V at 2 A, and 24 V at 1 A. The modular ac-to-dc supplies comply with international standards for safety and radiated noise.

Minimum input-to-output isolation is guaranteed at 3,750 V ac, and maximum leakage current is guaranteed at 5 μA. Also, the output is protected against short circuits and overvoltage. Unit prices for the line, which is available now, start at $156.

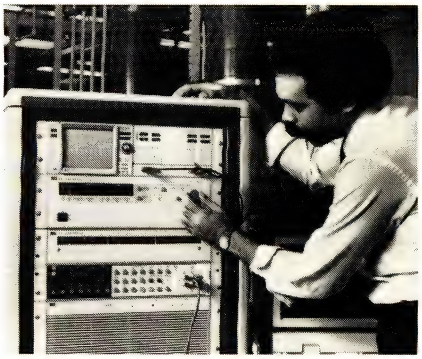
Analog Devices Inc., 2 Technology Way, Norwood, Mass. 02062. Phone (617) 329-4700
[Circle 402]

1,000-W supply produces 50 A at outputs of up to 20 V

The HP 6032A, a 1,000-W autoranging power supply, has features designed to satisfy the component burn-in and qualification, intelligent burn-in, laboratory, and automated-test equipment markets. Directly programmable through an IEEE-488 bus, the supply produces up to 50 A at outputs of up to 20 V and develops no fewer than 1,000 W through its 20-to-60-V range.

Using the unit, a programmer can confirm all programmed functions and values, as well as the status of output-voltage, current, and power supply. Software modification is easy because the programming format is self-documenting.

Its protection features include an over-voltage circuit and an operat-



ing-mode crossover-foldback feature that prevents damage to test fixtures from excessive currents.

The supply is priced at $3,100; delivery is estimated at six weeks.
Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Rd., Palo Alto, Calif. 94303 [Circle 403]

Switchers have a 250,000-h mean time before failure

The Reliatron EY series switching power supply meets all the specifications of Lambda's LU series of supplies, is physically and electrically interchangeable with the LUs, and in large original-equipment-manufacturer quantities is 15% less expensive than the LUs, says their maker.

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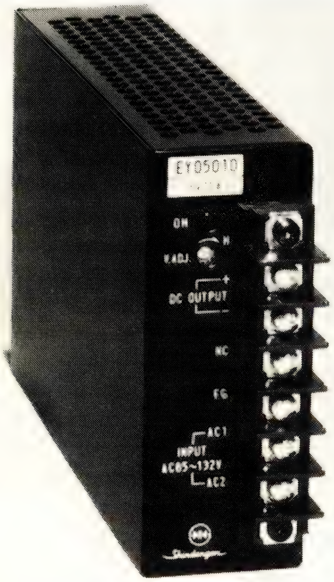

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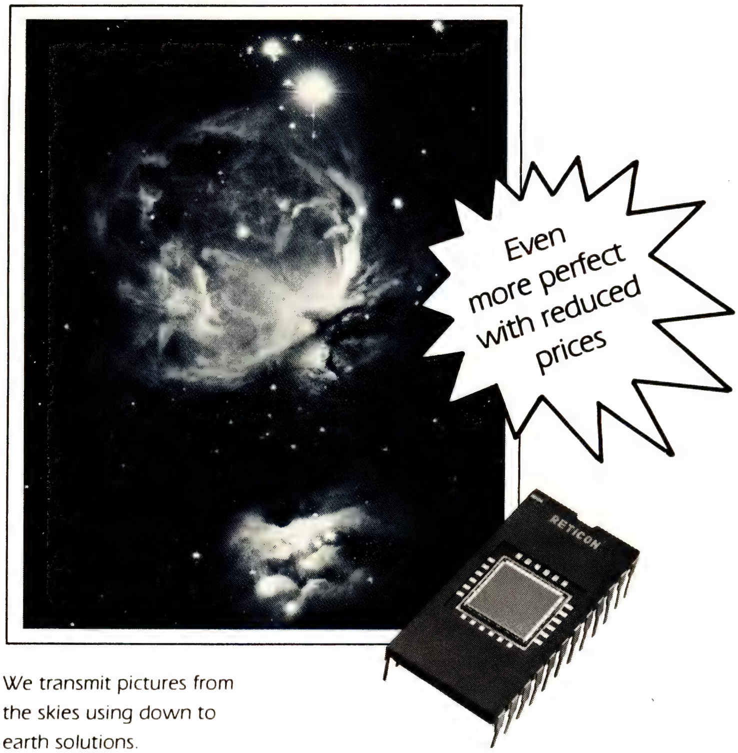

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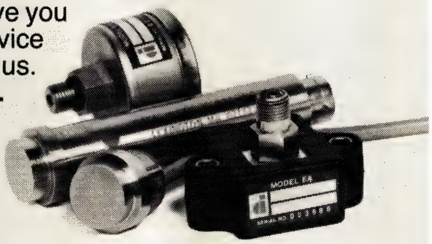

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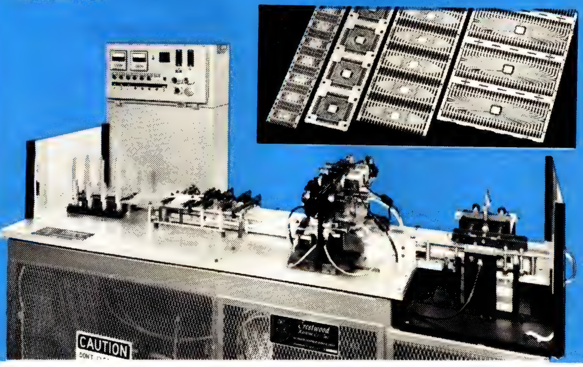

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Calex Manufacturing Inc., 3355 Vincent Rd., Pleasant Hill, Calif. 94523. Phone (415) 932-3911 [Circle 404]

16-W supply combines linear and switching techniques

A triple-output power supply rated at 16 W first uses a linear transformer to drop incoming line voltages to 18 V ac, then a switcher to supply regulated low-voltage dc current. The supply is designed for use with such units as computer peripherals, modems, microprocessors, telecommunications, and test devices.

Its input is 100/130 V at 60 Hz. Outputs are 2 A at 5 V dc, 0.250 A at 12 V dc, and 0.250 A at –12 V dc. The supply has built-in protection against overcurrent and short circuits, and meets Federal Communications Commission and Underwriters Laboratories requirements. Its operating range is from 0° to 50°C.

Available in 14 weeks, the supply is priced at $88.30 in quantities up to nine and $55.95 for 100 to 249 units.

Ault Inc., 1600 Freeway Blvd., Minneapolis, Minn. 55430. Phone (612) 560-9300 [Circle 405]

Efficient 50-W switchers have a 100-KHz operating frequency

The Alpha series of 50-W switching power supplies have a 100-KHz operating frequency and are suited for computer, industrial-control, and instrumentation applications. Features include soft start, isolated output, and up to 85% efficiency. The supplies conform to Federal Communications Commission and Underwriters' Laboratories standards.

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Energetec Systems Inc., Executive Plaza, 510 N. Church, Rockford, Ill. 61103. Phone (815) 962-0615 [Circle 407]

Semiconductors

C-MOS RAMs boast 100-ns access times

Using a complementary-MOS technology developed exclusively for fast dynamic memories, Intel Corp. is offering two versions of a 64-K-by-1-bit random-access memory. The 51C64 features a high-speed paging mode, dubbed Ripplemode by Intel, while the 51C65 has a static column-addressing scheme, which essentially makes the dynamic RAM act more like a static RAM.

Both chips—measuring 141 by 214 mils—are fabricated from Intel's high-performance complementary-MOS technology (C-H-MOS), which has minimum channel lengths of 1.2 μm. It also has a 250-Å gate oxide. C-H-MOS and the high-performance chip addressing modes result in access times as short as 100 ns. In the active mode, the chip dissipates 35 to 37 mA. In standby, the dissipation is rated at 50 μA.

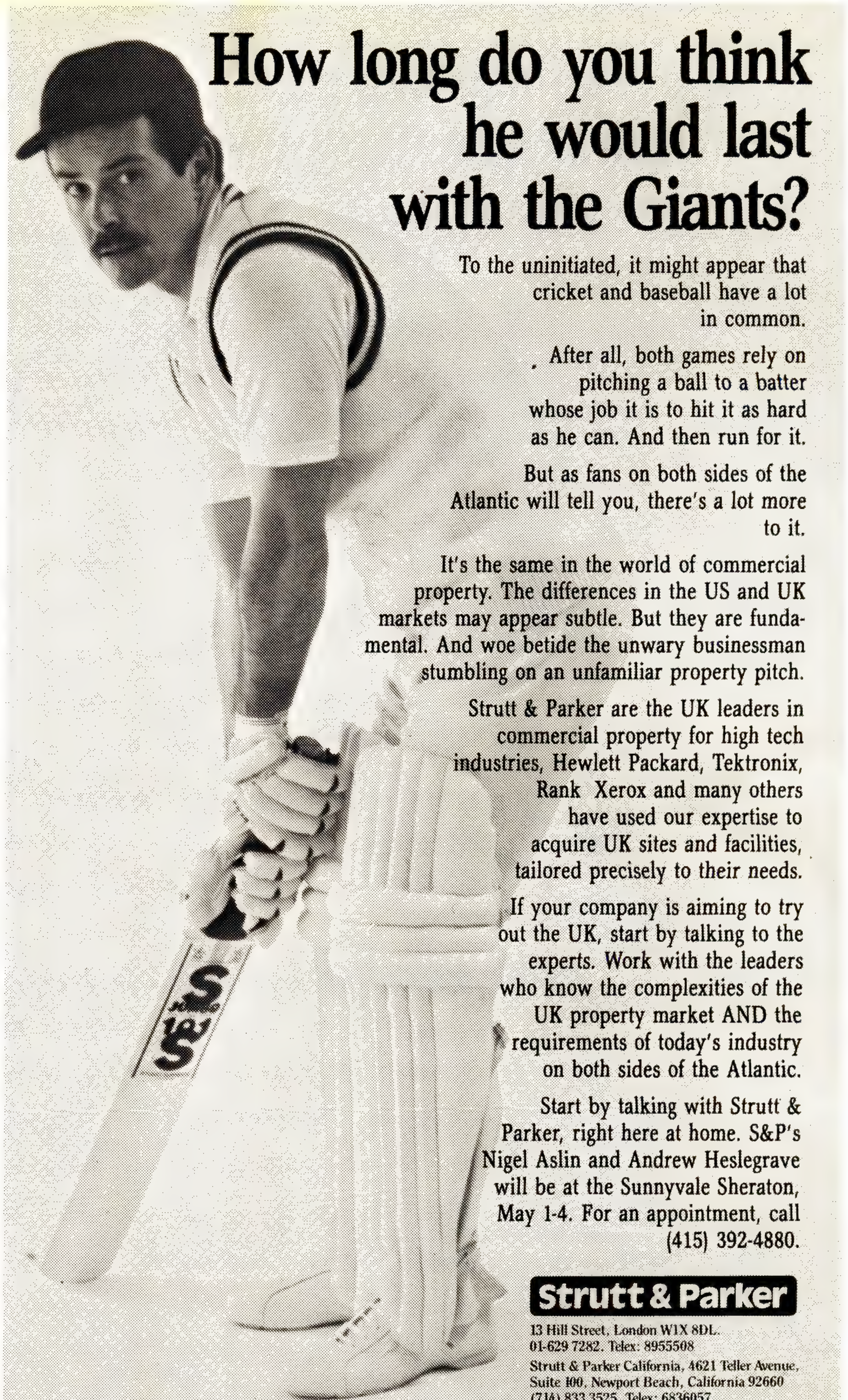
Immunity to soft errors is also enhanced by the new process because the memory array is isolated from the substrate using a buried n-well on a p-doped substrate. The technology lets Intel keep the die size small while increasing capacitance.

In quantities of 100, the 100-ns 51C64 Ripplemode 64-K device costs $20 each; the 51C65 static column-decode device costs $22 each. Both have 100-ns access times and use 4 mA at TTL levels on standby. Both are available immediately.

Intel Corp., Literature Department N-4, 3065 Bowers Ave., Santa Clara, Calif. 95051. Phone (503) 681-4212 [Circle reader service number 414]

256-K C-MOS E-PROM soon to be available

At February's International Solid State Circuits Conference in San Francisco, Seeq Technology de-



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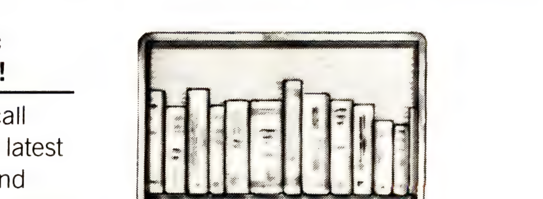

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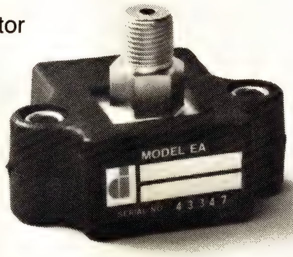

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scribed a 256-K complementary-MOS erasable programmable read-only memory built with 1.5-μm design rules. The 32-K-by-8-bit device had a cell size of 6 by 6.25 μm and 125-ns typical access times (200 ns over the whole military temperature range).

The chip has already been sampled to customers and will be shown at Electro as the 27C256, a product that Seeq says is the first commercially available 256-K E-PROM. The company is now in a preproduction phase and will begin full production in the third quarter of this year.

The chip utilizes an intelligent programming algorithm that programs all 256-K cells, in 8-bit chunks, in under a minute. The programmer exposes cells to a programming voltage for 1 ms, then checks to see if the programming took. If it did, the programmer fires another 4-ms burst, then moves on to the next byte; if not, additional 1-ms bursts are fired until a correct result is obtained.

The high cell density was achieved by the use of stepper-lithography and plasma-etching techniques, Seeq says. The p-channel devices are built in shallow 4-μm n-wells.

The circuit is packaged in the Jedec n-channel E-PROM format and replaces n-channel devices where lower power is required. Prices will be 10% to 20% higher than comparable n-channel MOS devices.

Seeq Technology Inc., 1849 Fortune Dr., San Jose, Calif. 95131. Phone (408) 942-1990
[Circle 339]

Chips combine output latches and bus transceivers

Two 74HCT/LS chips combine bus transceivers with output latches to facilitate high-speed multiplexed data transmission. The two chips—the ZX74HCT for transmitting noninverted data, and the ZXT4HCT/LS648 for *inverted* data—operate with a maximum propagation delay of 25 ns and 80 μA quiescent supply current. Both are TTL-equivalent, providing 12 mA of drive current at 0.4 V, and 24 mA at 0.5 V.

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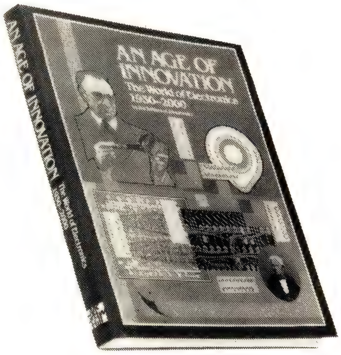

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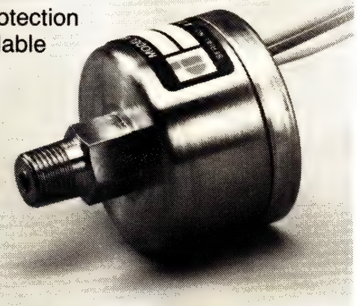

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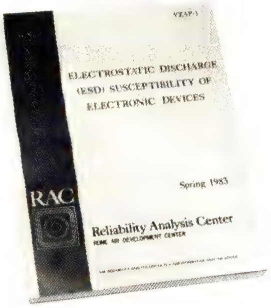
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the parts' data-source–selection lines, either part can serve as latched or unlatched transceivers, or both. The chips offer six control inputs—output enable, direction, two clocks, and two for data-source selection.

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Zytrex Corp., 750 E. Arques Ave., Sunnyvale, Calif. 94086. Phone (408) 733-3973
[Circle 412]

C-MOS static RAMs come in 200, 150, 100-ns versions

The 21C14 line of 4-K complementary-MOS static random-access memories are drop-in replacements for μPD444s and 5114s and are similar to synchronous types 6514 and 4344.

Available in speeds of 200, 150, 120, and 100 ns, the RAMs feature 35-mA operating current, 50-μA standby current, asynchronous operation, TTL compatibility, and 2-V data retention.

The RAMs are priced at $3.37 per unit in 1,000-piece quantities and can be delivered in 12 weeks.

Solid State Scientific, 3900 Welsh Rd., Willow Grove, Penn. 19090. Phone (215) 657-8400
[Circle 411]

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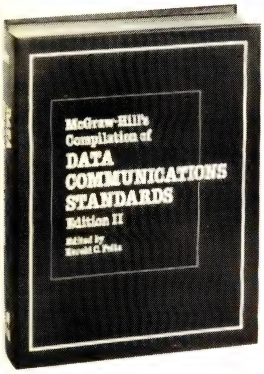

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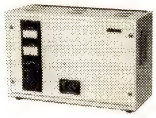

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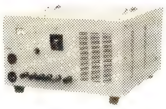

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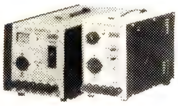

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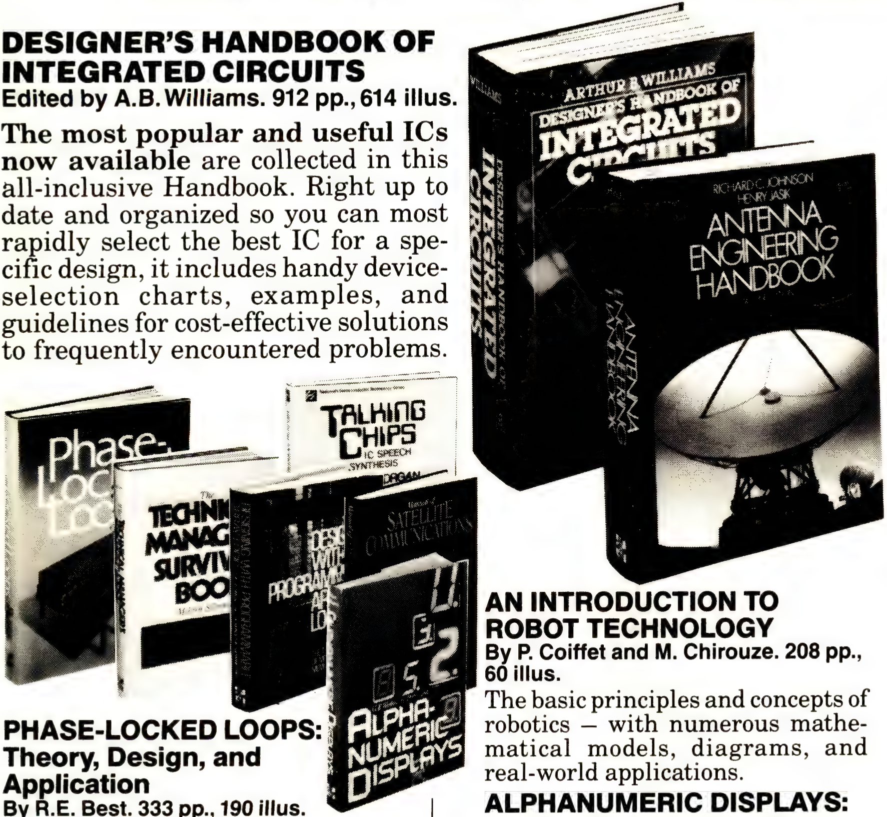

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Products newsletter

Motorola offers 6804 in smaller, 20-pin DIP

Ever since Motorola Inc. announced its MC6804 microcomputer, in late 1982, the chip has been one of the smallest in 8-bit markets. Now the company is making the 6804 available in a smaller package as well. First introduced in a 28-pin, 600-mil-long dual in-line package [*Electronics*, Dec. 15, 1982, p. 48], **the high-performance n-channel MOS 6804 is now also available in a 20-pin 300-mil DIP,** with eight fewer input/output ports. The 20-pin 6804—made from the same die as the 28-pin microcomputer—is aimed at system designs constrained by limited board space. At $1.50 to $2 each in high-volume quantities, the 20-pin chip's price is nearly the same as the 28-pin 6804.

Darlingtons use diodes for fast turn-off times

Rated at 15 A and 500 V, a line of PTC 6000 Darlington transistors is available from the Electronics Group of Allen-Bradley Co., in Torrance, Calif. The company says **the triple-diffused high-temperature glass-passivated mesa components provide fast-switching high-power performance** for switching power supplies, regulators, inverters, deflection circuits, and pulse-width-modulation system-control circuitry. An internal diode in the design allows the devices to be turned off quickly. In 100-piece quantities, the devices cost $5.50 each.

Stand-alone tape streamer holds 20 to 60 megabytes

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Programming tool boasts three-layered security

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Chassis accommodates 20 double VME cards

A VMEbus chassis from Data-Sud Systems/U. S. Inc., of Tempe, Ariz., accommodates up to 20 double Eurosize boards. **Two versions, table-top and 19-in. rack mount, include the cabinet, rack, VME motherboard, power supply, and fans.** Both come with two cooling fans and have a high-performance switching power supply. The motherboard provides transfer rates up to 20 MHz, as well as a daisy-chain system for interrupt and bus arbitration. A companion unit holds as many as nine VME boards. Also available are table-top versions that have positions for mounting two half-height 8-in. floppy-disk drives. Delivery is from stock and pricing starts at $1,995.

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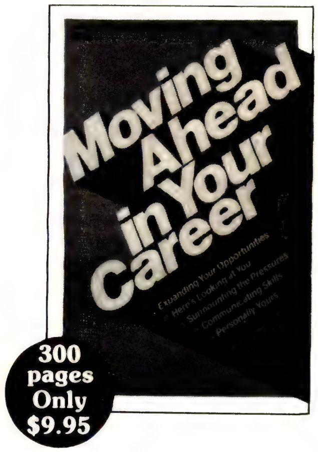
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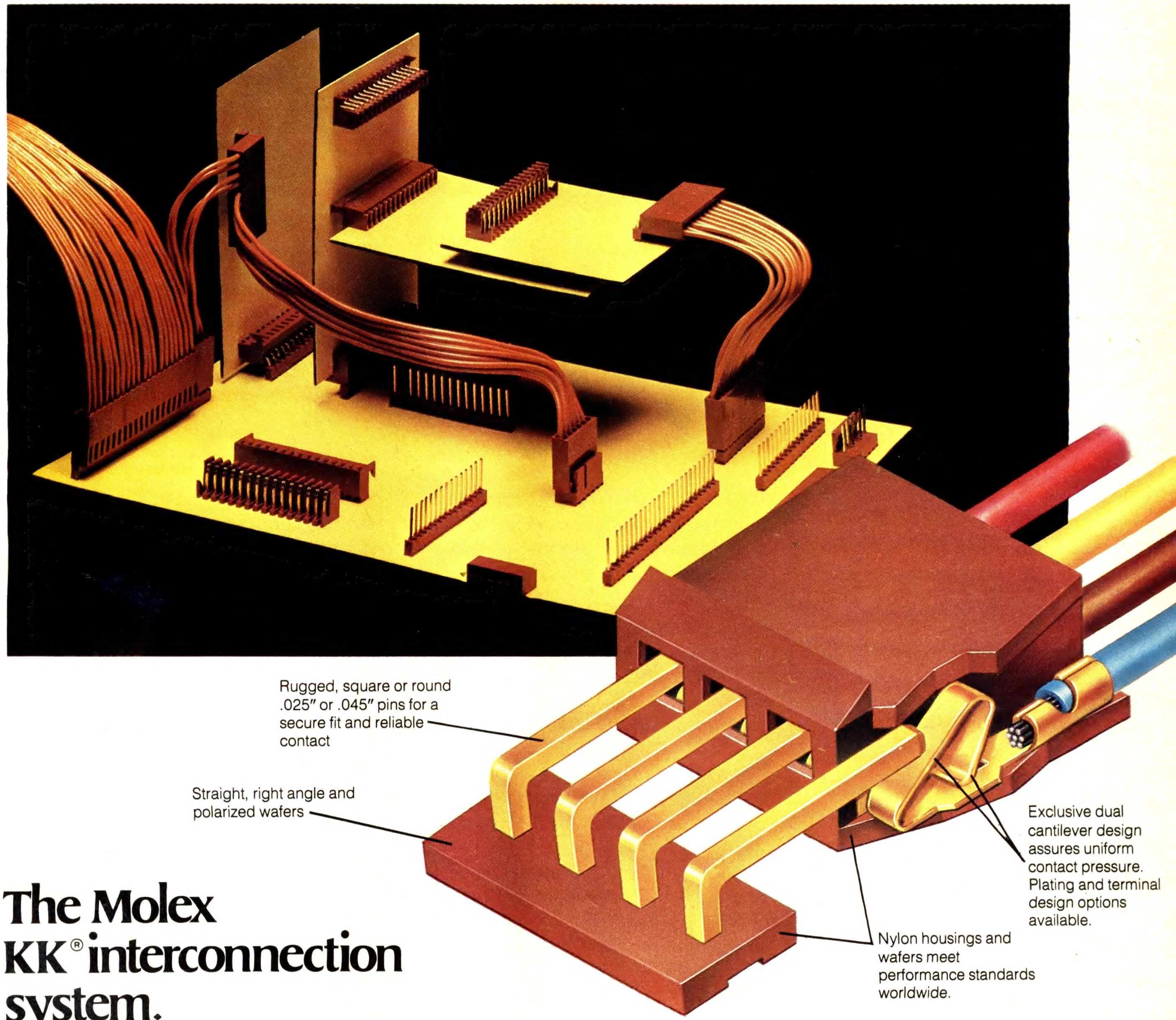
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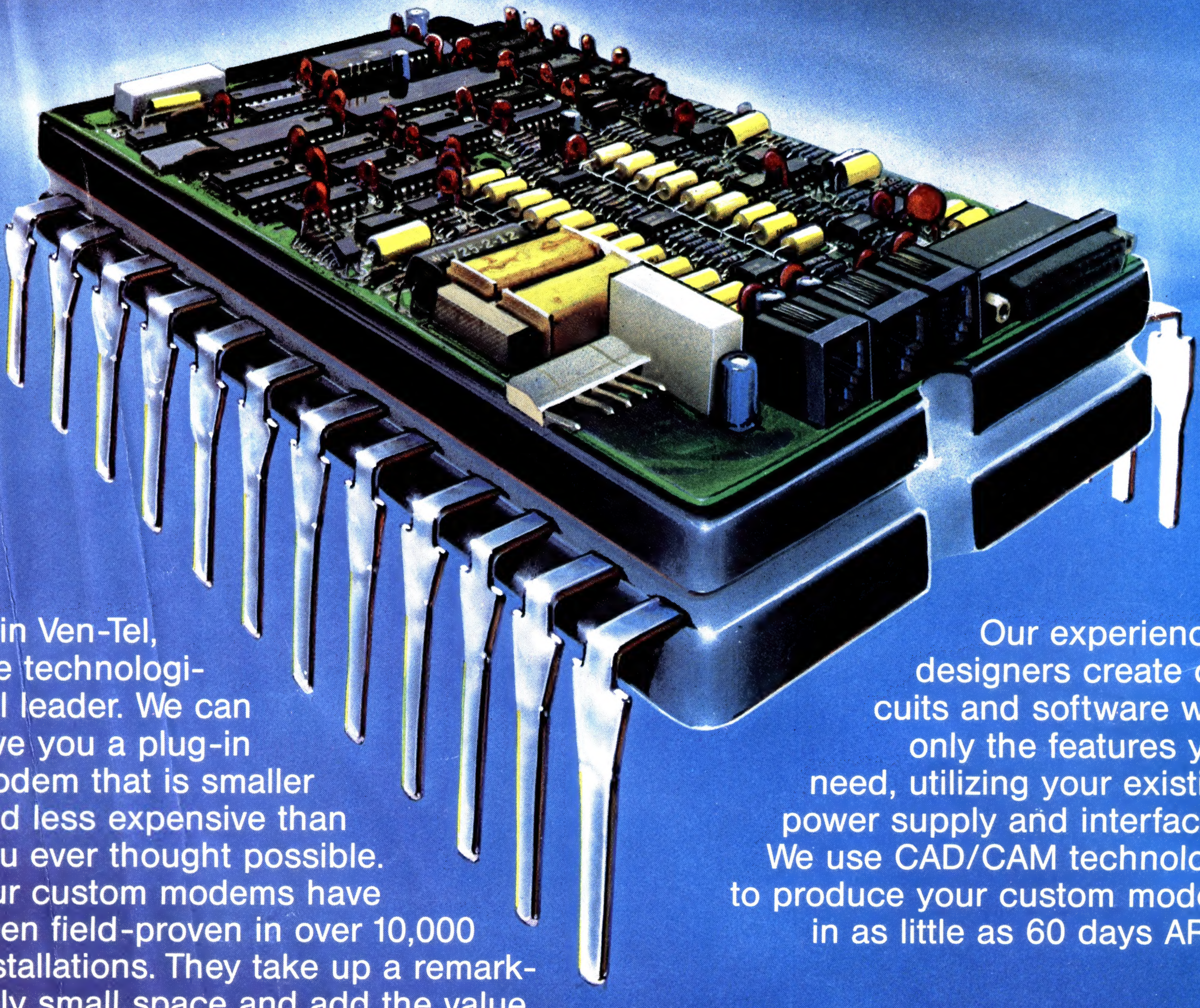

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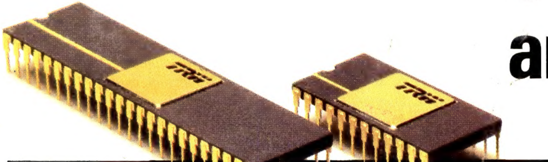

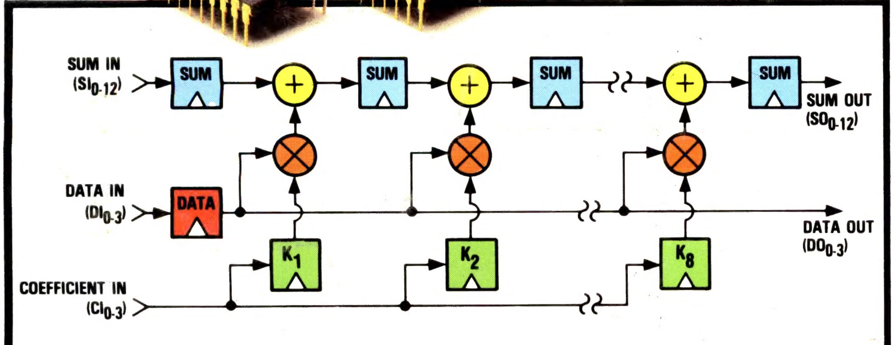

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